27.3 A 3MPixel Low-Noise Flexible Architecture CMOS Image Sensor

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Most active pixel CMOS image sensors use a source follower in the pixel circuit as shown in Fig. 27.3.1. However, the standard 3T pixel architecture typically has poor low-light sensitivity due to the large reset noise. 4T pixels incorporating a pinned diode have gained popularity due to low reset noise and dark current [1, 2]. However, pinned diodes require special technology development and may compromise device yield and reduced fill factor. In this paper, a 3T pixel image sensor with low reset noise, good fill factor, and flexible operation is described. The pixel architecture allows reset-noise reduction by negative feedback [3, 4] and increased responsivity in low-light conditions. Figure 27.3.2 shows the schematic of the new active pixel. The circuit inside the dashed box represents the pixel circuit. M_1 is the reset transistor, M_2 is the sense transistor, and M_3 is the row select (RS)/cascode transistor. Notice that the RS transistor M_3 is on the drain side of the sense transistor M_2. The current source, I_{col1}, is connected to the column line Col1. Another current source I_{col2} is connected to the second column line Col2. Column switches S_1 and S_2 connect the column lines to voltages V_1 and V_2, respectively, when they are on. For example, V_1 can be set at V_{DD} and V_2 at ground. With S_1 on and S_2 off, M_2 and I_{col2} function as a source follower. With S_1 off and S_2 on, M_2 and I_{col1} function as a common-source (CS) amplifier. In addition, biasing the gate of the row-select transistor at a lower voltage than V_{DD} allows a cascode amplifier configuration that further reduces the reset noise as explained later.

In the CS configuration, the drain of M_2 is connected to I_{col1}, its source is connected to V_2, i.e., ground. When the row-select signal, RS, is high, the RS transistor M_3 is turned on, and the sense transistor M_2 and the I_{col1} behave as an actively loaded CS amplifier. The input of the CS amplifier is the sense node (Node 1), and the output of the amplifier is the column line Col1. During the reset phase, the row-select signal goes up turning on the row-select transistor M_3. The reset signal, RESET, also goes high to a reset voltage V_{RESET}, typically V_{DD}, turning the reset transistor M_1 on. M_1 provides negative feedback from the output of the CS amplifier to the input. Both the input and output voltages settle to a voltage $V_R=V_{GS2}$ where V_{GS2} is the gate-to-source voltage of M_2 at the drain current of I_{col1}. The reset is completed and the integration period begins when the reset signal returns low, turning off the reset transistor M_1. The row-select signal also goes low turning M_3 off. This turns the CS amplifier off, and another row can now be reset in the same manner.

During the integration period, the photo current is integrated on the sense-node capacitance C_S. At the end of the integration period, the row-select signal RS goes high again, turning the CS amplifier back on. Assuming the open-loop gain of the CS amplifier is large, the photo charge that is integrated on the capacitance C_S is completely transferred to the capacitance C_I between the gate and the drain of the sense transistor M_2. Typically, C_I consists of parasitic capacitance that already exists including the gate-to-drain capacitance C_{GD2} of M_2 and stray capacitance. The double-sampling (DS) circuit measures the difference between the output voltages of the CS amplifier immediately after the reset and at the end of the integration period. To avoid using frame buffers, the reset value of the next frame is used instead. It can be shown that this difference, photo response voltage V_p is:

$$V_p = \frac{I_P T_{INT}}{C_I}$$

Since C_I is significantly smaller than the sense capacitance C_S, the photo response voltage is higher for given photo current. Therefore, the responsivity of the image sensor is significantly improved compared with the source-follower mode. Thus, this mode is desired in low-light conditions, but the image saturates at a relatively low light level. Therefore, the source-follower readout mode is preferred in brighter conditions.

It is also noted that during the reset phase, if the bandwidth of the RC circuit given by the ON resistance of M_1 and the sense capacitance C_S is made significantly lower than that of the CS amplifier, the reset noise is effectively suppressed. This is because the CS amplifier, in conjunction with the negative feedback provided by M_1 corrects the noise at the sense node [4]. The bandwidth of the RC circuit can be made low by setting the reset voltage V_{RESET} such that the reset transistor M_1 is biased deep in the subthreshold region during the reset phase. Alternatively, the waveform of the reset signal RESET can be made to fall slowly at the end of the reset period so that the reset transistor is deep in the subthreshold region while the reset signal is lowered. It can be shown that the reset noise is reduced by the factor $\frac{C_S}{C_I}$.

The cascode mode further reduces the reset noise, because it removes the effect of C_{GD2} from C_I.

A 3MPixel image sensor employing this flexible architecture is implemented in a 0.18μm CMOS image sensor technology. The placement of the RS transistor on the drain side of the sense transistor enables a compact layout, providing 50% fill factor in a 2.54×2.54μm² pixel size. The imager supports up to 4:1 vertical and 2:1 horizontal analog binning to further reduce the noise in lower spatial resolution images.

Figure 27.3.3 shows a comparison between hard reset, hard-soft reset, and cascoded low-noise reset. In the hard and hard-soft reset mode, the pixel is operated in the source-follower mode for both reset and readout. In the low-noise cascoded reset mode, the pixel is reset in a common-source mode with the row-select transistor biased below V_{DD} to reduce the effect of C_{GD2}. The low-noise reset mode reduces reset noise by a factor of 2 compared with the standard hard reset. The cascoded low-noise reset mode further reduces reset noise by 10%.

Figure 27.3.4 and 27.3.5 compares the standard mode versus the common-source readout mode. The responsivity is increased by 5 folds compared to the source-follower readout mode. Column-parallel ADCs with a flexible timing control is integrated with maximum 12b resolution. This image sensor runs at a maximum of 30frames/s at full 3MPixel resolution with 100MHz clock input. The summary of the imager performance is given in Fig. 27.3.6. Figure 27.3.7 shows the chip micrograph.

References:

[1] H. Takahashi, et. al. "A 3.9μm Pixel Pitch VGA Format 10b Digital Image Sensor with 1.5 Transistor/Pixel," *ISSCC Dig. Tech. Papers*, pp. 108-109, Feb., 2004.

[2] M. Mori, et. al. "A 1/4in 2M Pixel CMOS Image Sensor with 1.75Transistor/Pixel," *ISSCC Dig. Tech. Papers*, pp. 110-111, Feb., 2004.

[3] B. Fowler, M. Godfrey, J. Balicki, and J. Canfield, "Low-Noise Readout Using Active Reset for CMOS APS," *Proc. SPIE*, vol. 3965, pp. 126-135, May, 2000.

[4] L. Kozlowski, et. al, "Progressive 1920×1080 Imaging System on- Chip for HDTV Cameras," *ISSCC Dig. Tech. Papers*, pp.358-359, Feb., 2005.

 1-4244-0079-1/06/$20.00

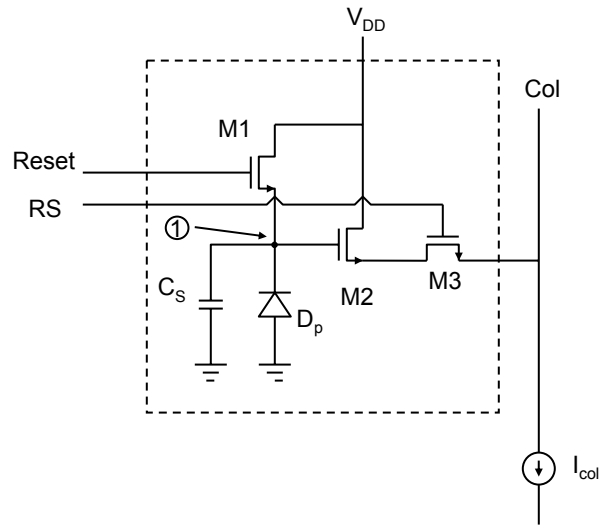


Figure 27.3.1: Conventional 3T pixel with source-follower readout circuit.

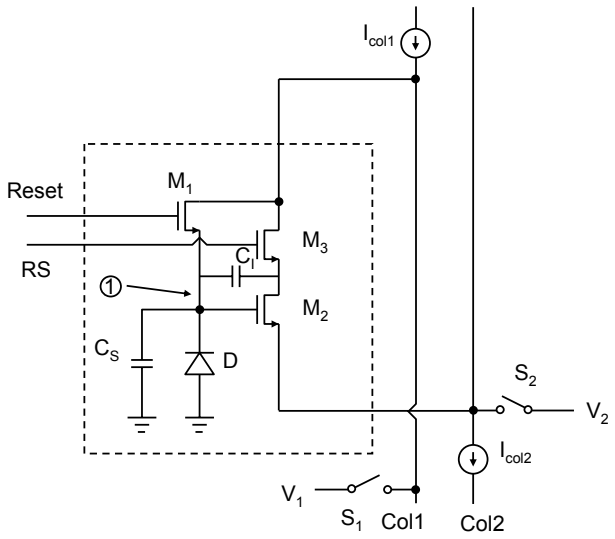
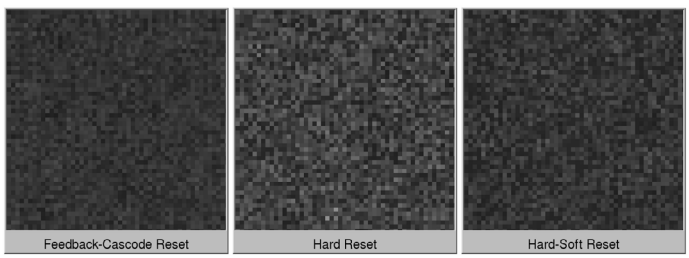


Figure 27.3.2: Proposed 3T pixel with flexible reset/readout circuit.



Temporal noise=13e⁻ Temporal noise=28e⁻ Temporal noise=19e⁻

Figure 27.3.3: Dark images with different reset modes (32x gain).

Figure 27.3.4: Sample Image - standard read mode (1000lux, 1/30s).

Figure 27.3.5: Sample Image – common source read mode (1000lux, 1/30s).

Parameter	Result	Unit
Die Size	6.1x6.5	mm^2
Technology	CMOS 0.18μm	
Pixel array	2140x1584	pixels
Pixel Size	2.54x2.54	μm^2
Max frame rate at full resolution	30	frames/s
Max ADC resolution	12	bits
Power consumption at 3MPixel 10b output	275	mW @ 30frames/s
Power consumption at 3MPixel 12b output	215	mW @ 15frames/s
Power consumption at VGA resolution	63	mW @ 30frames/s
Full Well Capacity	13K	electrons
Conversion gain	110	μV/e
Dark Temporal Noise in low-noise reset	13	electrons
Dark Temporal Noise in hard-soft reset	19	electrons
Dark Temporal Noise in hard reset	28	electrons
Dark FPN Noise @1/7 sec	10	electrons
Read Noise	3	electrons
Dark Leakage @24C	100	electrons/sec
Responsivity in SF mode@550nm	1.0	V/lux-sec
Responsivity in CS mode@550nm	5.0	V/lux-sec

Figure 27.3.6: Performance summary.

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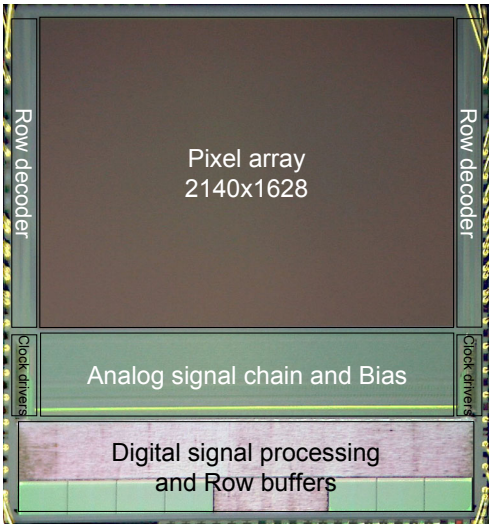

Figure 27.3.7: Chip micrograph.

