25.5 A Zero-Crossing-Based 8b 200MS/s Pipelined ADC

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Comparator-based switched-capacitor (CBSC) circuits were introduced in [1] as an alternative to opamp-based designs to overcome the limitations of opamps due to device and voltage scaling. Reduced device gain and signal swing make it increasingly difficult to design high-gain high-speed feedback loops with opamps. CBSC circuits replace the opamp with a comparator and a current source (see U_1 and I_1 in Fig. 25.5.1) to eliminate these difficulties and operate more power efficiently. Just as the opamp in an opamp-based design, the comparator contributes most significantly to the overall FOM in a CBSC design. Generally, a comparator must resolve the difference between 2 arbitrary voltages. The input of the comparator in a CBSC circuit, however, is not arbitrary but is a voltage ramp with a constant slope. Therefore, the comparator actually performs a zero-crossing detection. This work replaces the general-purpose comparator of CBSC circuits with a more power-efficient zero-crossing detector and demonstrates this architecture, zero-crossing-based circuits (ZCBC), with an 8b 200MS/s 1.5 b/stage [2] pipelined ADC.

The implementation of the zero-crossing detector and the complete pipeline stage is shown in Fig. 25.5.2. M_1 and M_2 make up a dynamic zero-crossing detector (DZCD). The timing diagram is shown in Fig. 25.5.4. The input voltage is sampled on C_1 and C_2 prior to the rising edge of ϕ_2. When ϕ_2 rises, the pre-charge signals (pc) and (pcb) initialize the charge-transfer phase by resetting node (V_o) low and node (V_p) high. This pushes the DZCD input node (V_x) down and turns off M_1. The output voltage V_o then begins to ramp pulling V_x with it. When V_x gets high enough to turn M_1 on, it pulls V_p low and stops the charge transfer by turning the sampling switch M_3 off. The DZCD would be unsuitable as a general-purpose comparator since the threshold depends on the input waveform. The threshold varies on a sample-to-sample basis if an arbitrary input waveform is applied. However, the ramp waveform in a ZCBC ensures a constant threshold.

The advantage of the DZCD over a traditional comparator is that it draws no DC bias current and consumes only the power necessary to switch the output node (Vp) when the input crosses the threshold. Thus, the entire ADC draws no DC current, consumes only CV^2f power, and makes a single ramp as power efficient as the dual-ramp scheme proposed in previous CBSC circuits. A single ramp simplifies the implementation and enables higher speeds. One drawback of the DZCD is that the threshold is a function of ramp rate, process, and temperature. For this initial design an auto-zeroing mechanism to null these dependencies is not implemented. The implementation of auto-zeroing, however, would be straightforward. Another drawback is the single-ended nature of the circuit, which makes it unsuitable for high-resolution circuits.

As the ramp rate increases to enable faster operation, so does the current through, and the voltage across all the switches. At high current levels, the non-linear resistance typical of the CMOS switches S_1, S_2, and S_3 of Fig. 25.5.1 can cause linearity problems at the output. These series switches, however, can be removed by splitting the current source up to charge each capacitor separately as shown in Fig. 25.5.2. Switches S_5 and S_6 are added to remove ramp-rate mismatch between the 3 legs and only carry small amounts of current. Since all other switches are connected to DC voltages, the voltage drop across them will be constant and will not affect the linearity.

A further technique in this design is in the implementation of the bit-decision comparators (BDCs). The BDCs perform a coarse quantization of the output voltage V_o. Traditionally they are implemented as clocked-comparators as shown in Fig. 25.5.1. In a single-ramp ZCBC implementation, they must make their decision before the ramp can begin, and this delay reduces the available time for the DZCD. To remove the BDC from the critical path and eliminate the associated speed burden, a different approach is used in this design. Since the output voltage V_o ramps linearly until the DZCD trips, the time at which the DZCD trips is proportional to output voltage. Therefore, in a manner analogous to a single-slope ADC, sampling the DZCD output with flip-flops whose clock is phase-aligned with the decision threshold yields an equivalent coarse quantization of the output voltage. Since the ADC input drives the first stage, such bit decisions are not possible for the first stage. Thus traditional clocked comparators are used for the first stage and the input sampling period of the passive MOSFET-C sampler is reduced to give them ample time to make their decision.

To generate the clock phase that corresponds to the desired $\pm V_{ref}/4$ bit-decision voltages necessary for a 1.5b/stage ADC, the circuit of Fig. 25.5.3 is used. The timing diagram is shown in Fig. 25.5.4. The transfer phase clock ϕ_2 goes through a voltage-controlled delay line (VCDL) and produces ϕ_{BD}. ϕ_{BD} along with the bit-decision voltage $V_{ref}/4$ goes into a replica pipeline stage. The output bit of the replica stage is then fed back to the VCDL to adjust the phase of ϕ_{BD} for the next sample. The actual circuit implementation of the VCDL is also shown in Fig. 25.5.4. A current-starved inverter consisting of M_1, M_2, and M_3 controls the delay. If capacitor C_3 starts fully charged to give the VCDL minimal delay, the BDC in the replica stage samples the DZCD output immediately to yield a high decision output Q. Q then feeds back into the VCDL and produces a down signal D to short capacitors C_2 and C_3. As C_2 was previously shorted to ground, the voltage on C_3 decrements and the delay increases. The delay continues to increase each sample until the BDC output Q in the replica stage goes low and thus generates an up signal U to short C_1 to C_3. Since C_1 was previously fully charged, the C_3 voltage will increment and shorten the delay. In steady-state the output bit Q toggles high and low to keep ϕ_{BD} at the right location. The small amount of jitter from such toggling is not an issue due to the over-range protection offered by a 1.5b/stage ADC. Two bit-decision phases are necessary to provide the $+V_{ref}/4$ and $-V_{ref}/4$ phases. For area and power savings, a single replica ADC stage is toggled between $-V_{ref}/4$ and $+V_{ref}/4$ and 2 VDCLs.

This design is implemented in a 0.18μm CMOS technology in an active die area of $0.05mm^2$ (Fig. 25.5.7). Figure 25.5.5 shows the DNL is within ±0.75LSB and the INL within ±1.0LSB at 200MS/s. Figure 25.5.6 shows the frequency response, power consumption, and FOM at various sampling frequencies. The ENOB is 6.9b and 6.4b at 100MS/s and 200MS/s, respectively. The power consumption, which consists entirely of dynamic CV^2f power, at 200MS/s is 8.5mW (2.9/5.6mW analog/digital) from a 1.8V supply. The corresponding FOM is 380 fJ/step at 100MS/s and 510 fJ/step at 200MS/s respectively.

Acknowledgments:
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References:
[1] T. Sepke, J. K. Fiorenza, C. G. Sodini, et al., "Comparator-Based Switched-Capacitor Circuits for Scaled CMOS Technologies," *ISSCC Dig. Tech. Papers*, pp. 220-221, Feb., 2006.
[2] S. H. Lewis, H. S. Fetterman, G. F. Jr., Gross, et al., "A 10-b 20-Msample/s Analog-to-Digital Converter," *IEEE J. Solid-State Circuits*, vol. 27, pp. 351-358, Mar., 1992.

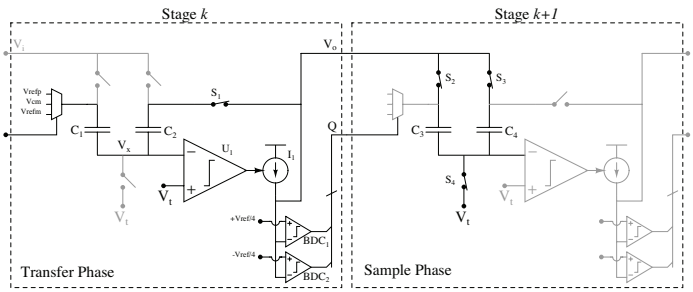

Figure 25.5.1: Two stages of a 1.5b/stage CBSC pipelined ADC. U_1 and I_1 perform the equivalent functionality of an opamp.

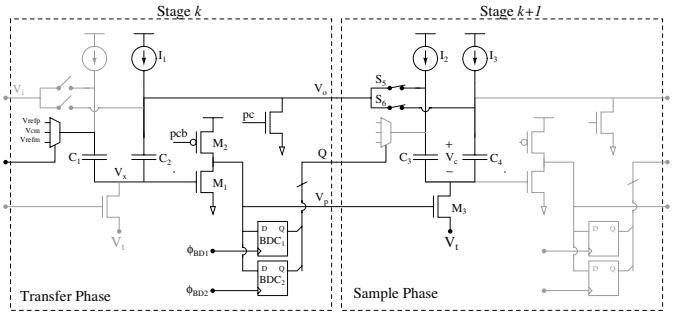

Figure 25.5.2: Implementation of 2 stages of the 1.5b/stage ZCBC pipelined ADC.

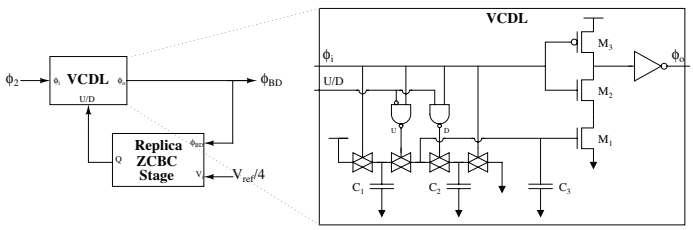

Figure 25.5.3: Block diagram of the feedback loop that generates ϕ_{BD} for the bit-decision flip-flops. The VCDL implementation is also shown.

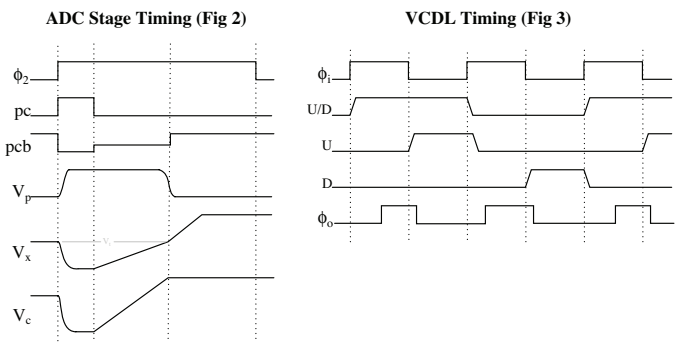

Figure 25.5.4: Timing diagrams for ADC pipeline stage and VCDL feedback loop.

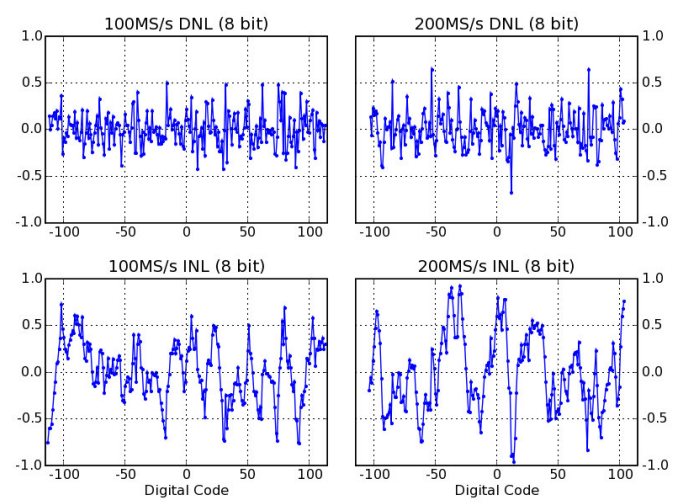

Figure 25.5.5: DNL and INL plots for 100MS/s and 200S/s operation.

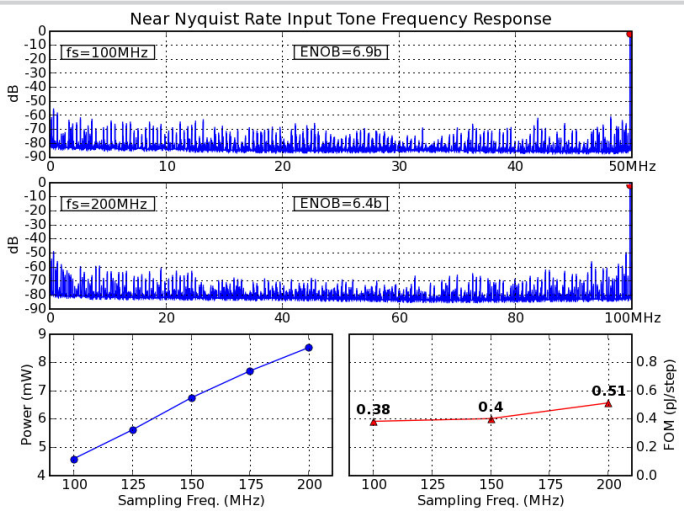

Figure 25.5.6: Frequency response for 100MS/s and 200MS/s operation. Power consumption versus sampling frequency. FOM versus sampling frequency.

Continued on Page 615

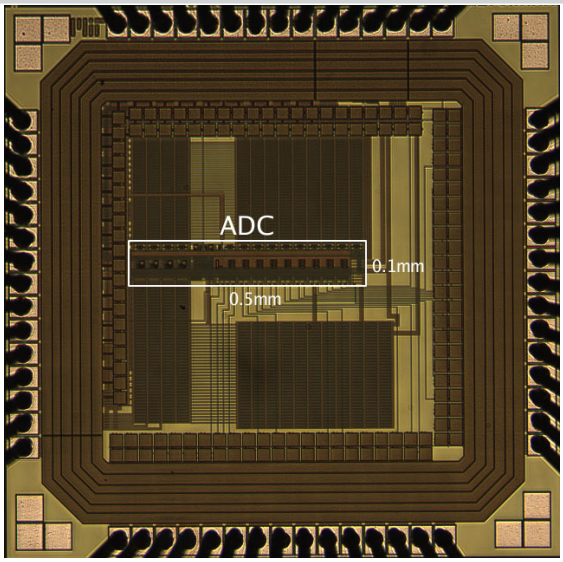

Figure 25.5.7: Die micrograph in 0.18µm CMOS.

