25.5 A Zero-Crossing Based 8b, 200MS/s Pipelined ADC

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Outline

- Motivation
- Review of Op-amp & Comparator-Based Circuits
- Introduction of Zero-Crossing Based Circuits
- Implementation Details
- Performance Results
- Conclusion

Motivation

- Technology scaling is making opamp-based SC circuit design increasingly difficult
- Op-amp design issues
  - **Decreasing voltage supplies**
    - Reduces signal swing
    - Requires increase in capacitance to maintain SNR
  - **Decreasing intrinsic device gain**
    - Cascode gain stages
      - Exacerbates low swing problem
    - Cascade gain stages
      - Stability versus bandwidth/power tradeoff

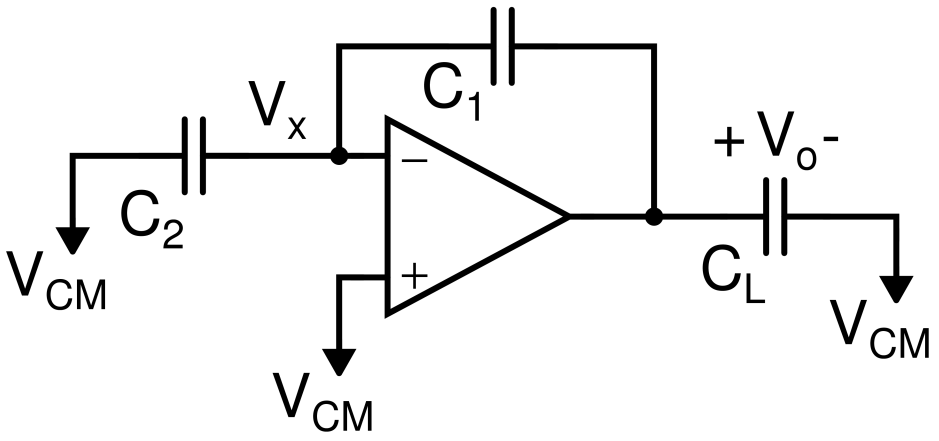
Comparator Based Circuits

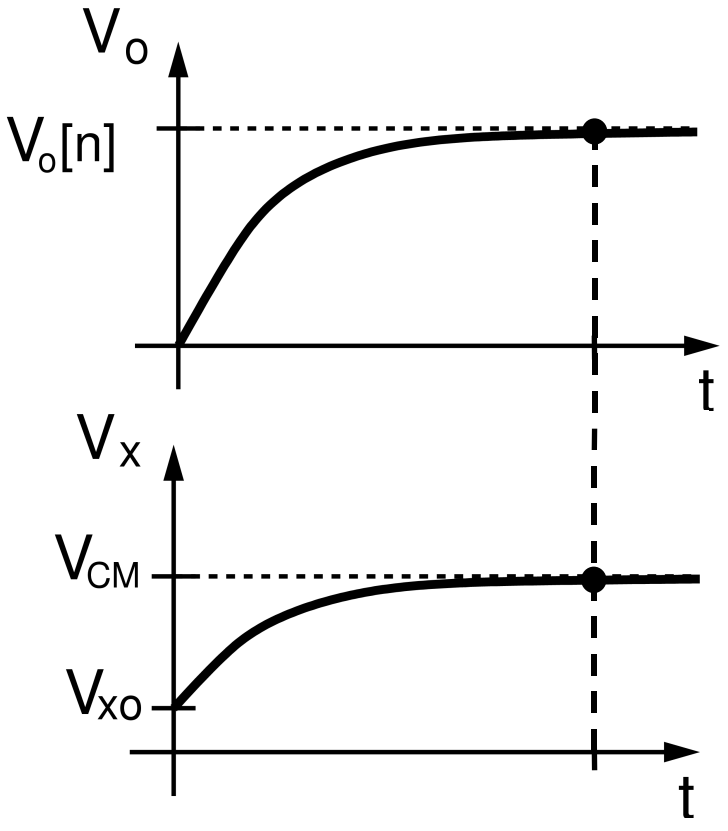
- **Comparator Based Switched Capacitor[1] (CBSC) Circuits:**
  - Eliminate op-amps and stability issues
  - Utilize architectures similar to op-amp based circuits
    - Works with ADCs, DACs, Filters, Amplifiers, etc.
  - Amenable to scaled technologies
  - Operate more power-efficiently

1. T. Sepke, et. al., “Comparator-based switched-capacitor circuits for scaled CMOS technologies,” ISSCC 06.

Op-amp Based Switched-Capacitor Charge Transfer Phase

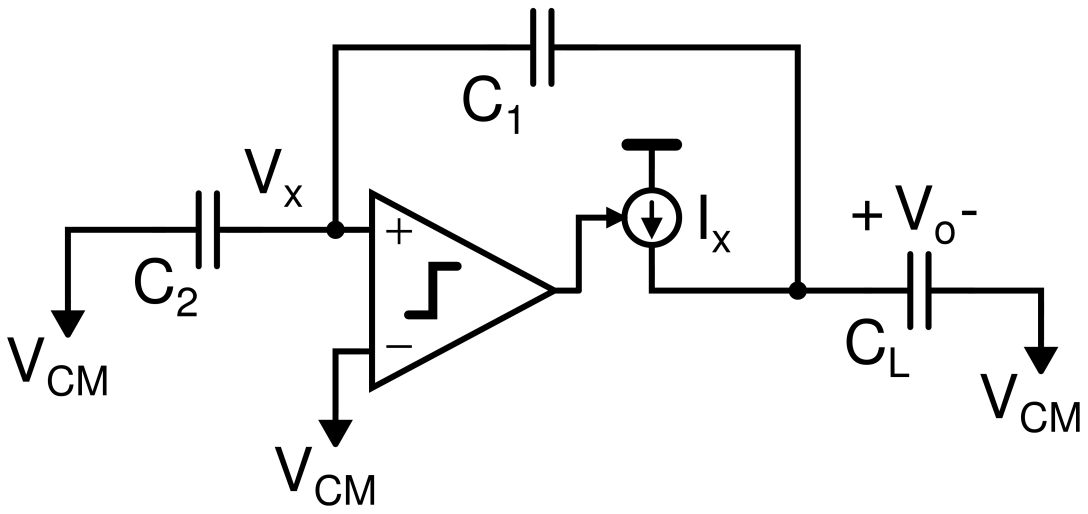
- Op-amp **forces** virtual ground condition
- Exponential settling to virtual ground

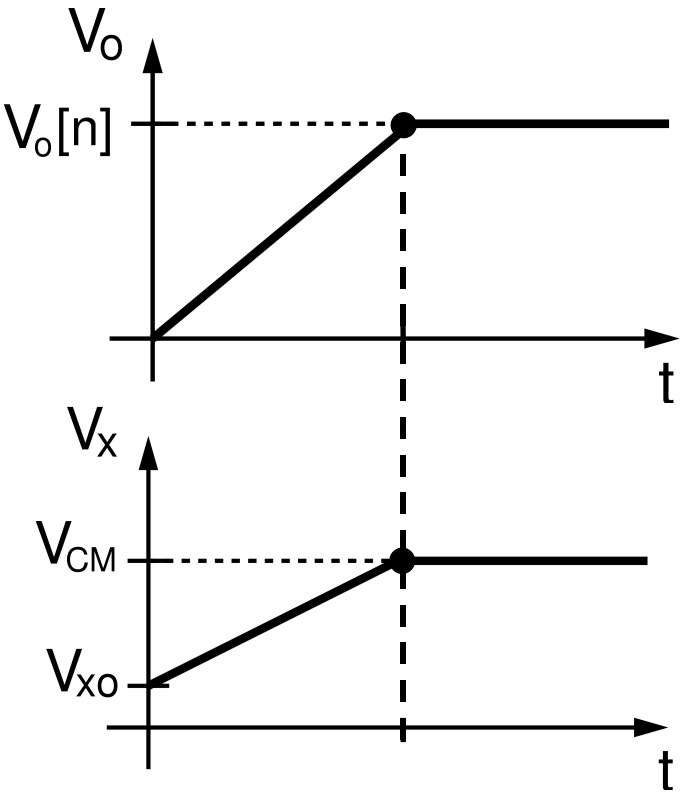




Comparator-Based Switched-Capacitor Charge Transfer Phase

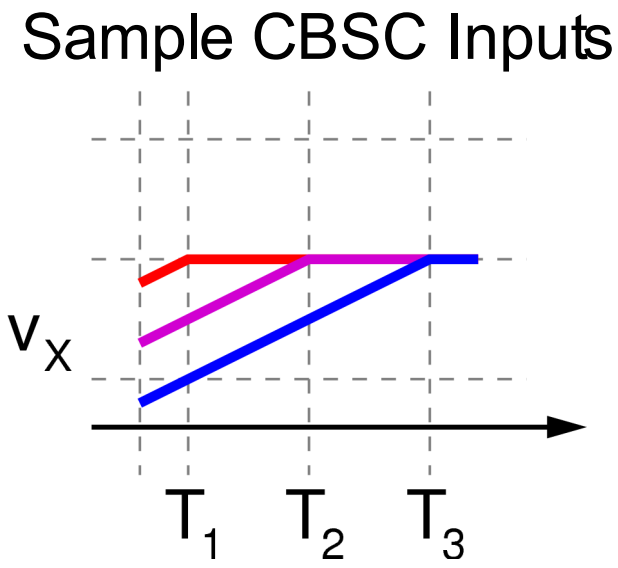
- Current source sweeps the output voltage
- Comparator **detects** virtual ground condition and turns off current source
- Correct output voltage is sampled on C_L





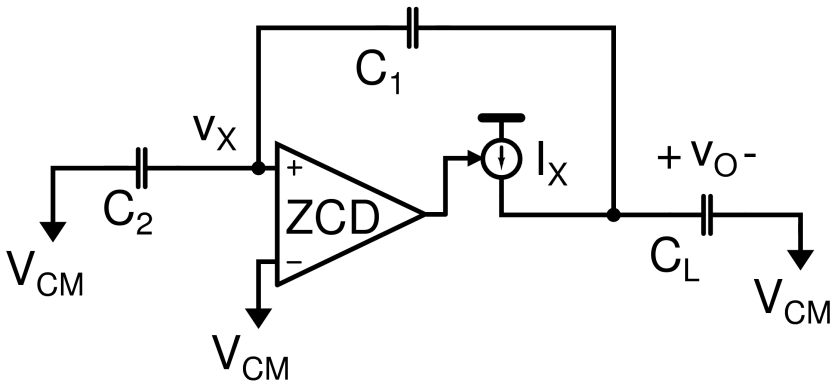
CBSC Observation

- A general purpose comparator must compare two arbitrary voltages
- CBSC comparators:
  - Do not have arbitrary inputs
  - Have inputs that are constant slope voltage ramps
  - Perform a **zero-crossing detection**



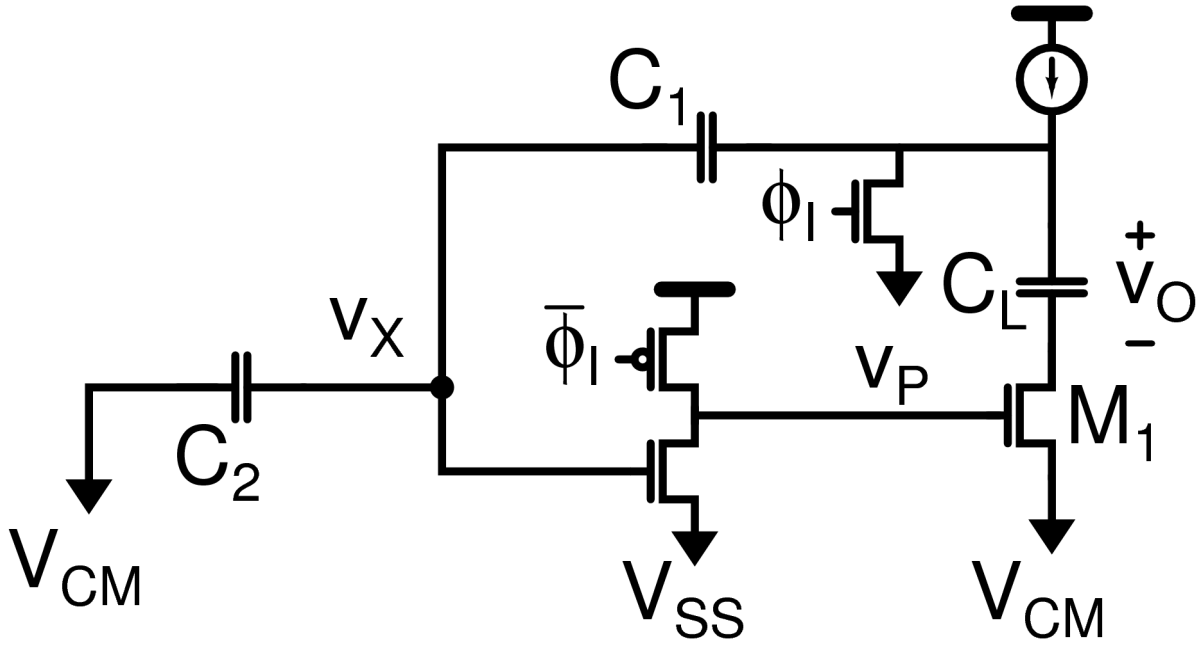
Zero-Crossing Based Circuits (ZCBC)

- CBSC circuits generalize to Zero-Crossing Based Circuits (ZCBC)
  - Zero-Crossing Detector (ZCD) replaces comparator



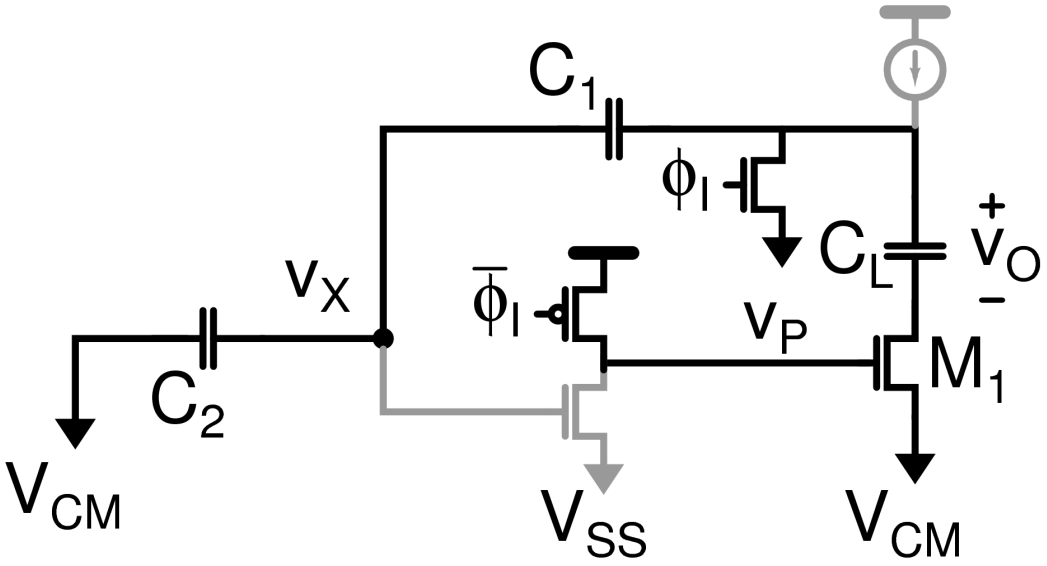
Dynamic ZCBC Transfer Phase

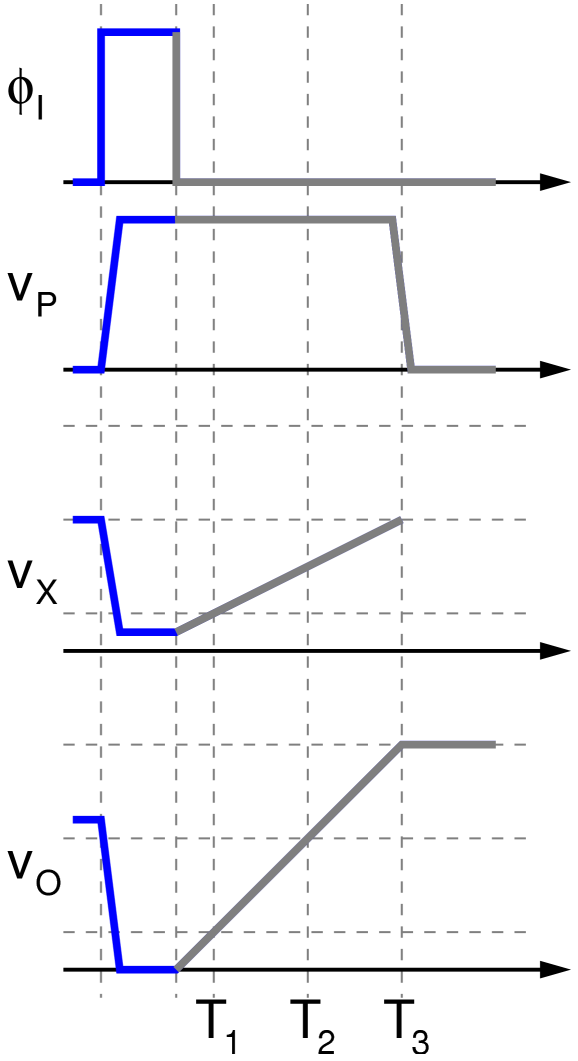
- C_1 and C_2 sample the input signal in a previous sampling phase
- **Transfer phase goal**: Charge C_L to the voltage that realizes the virtual ground condition on v_X



Dynamic ZCBC Implementation

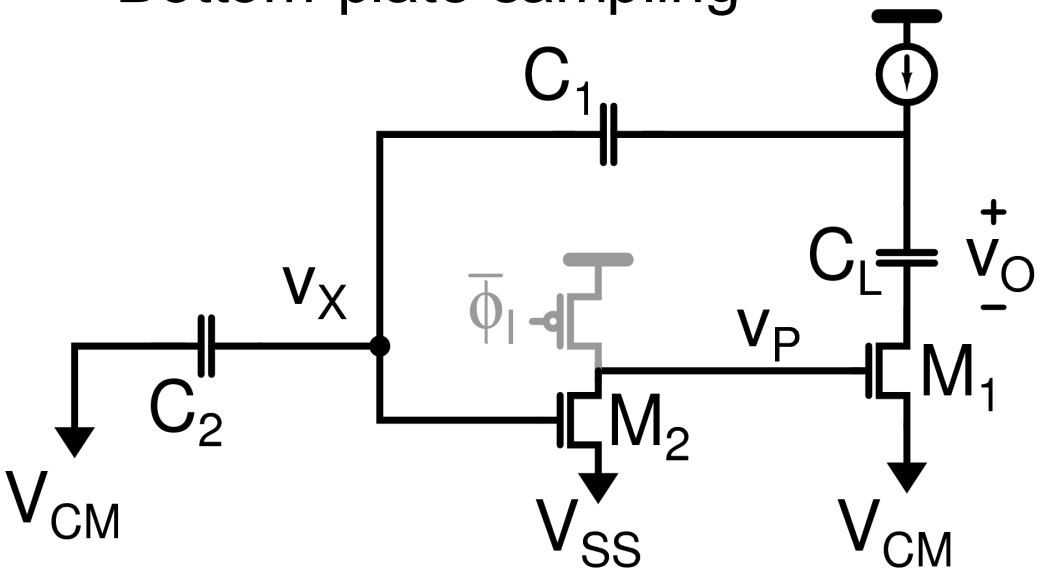
- ϕ_I initializes charge transfer
  - v_P gets reset high
  - v_O gets reset low
  - v_X gets pushed down

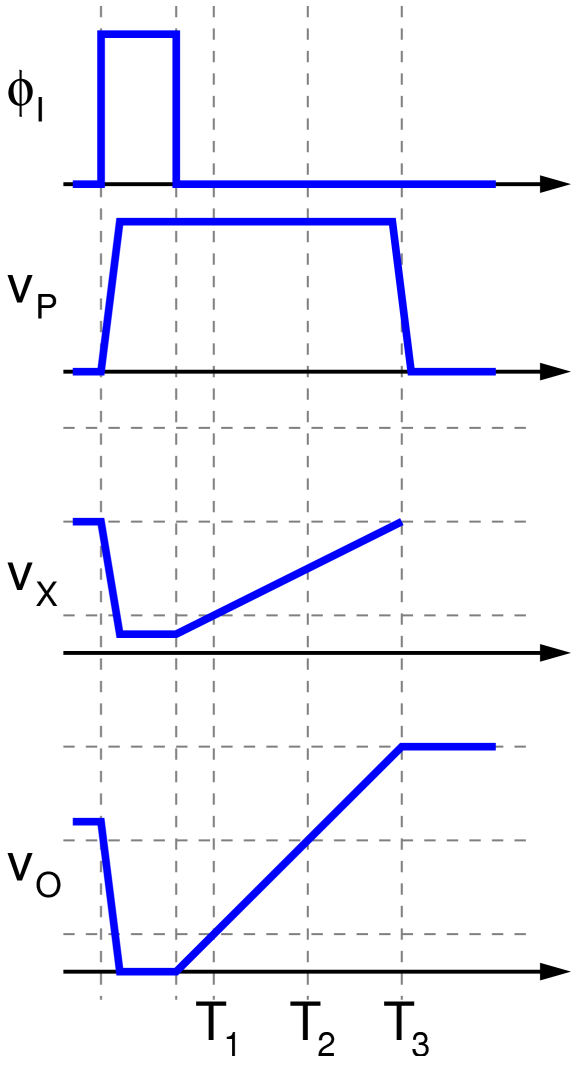




Dynamic ZCBC Implementation

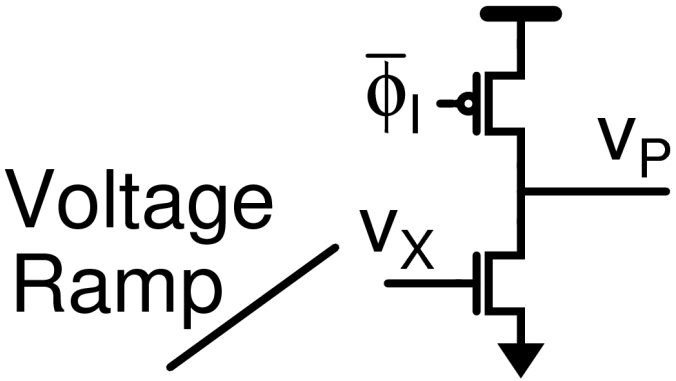
- Current source turns on
  - $\mathbf{v_o}$ and $\mathbf{v_x}$ start ramping
- $\mathbf{v_x}$ ramps until it turns on M_2
  - M_2 pulls $\mathbf{v_P}$ low
  - Sampling switch M_1 turns off
  - Bottom-plate sampling





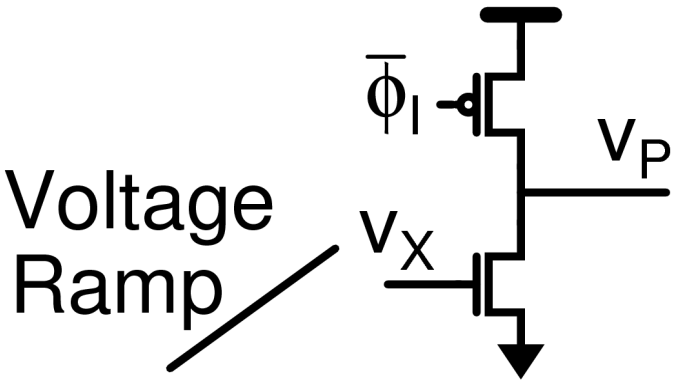
Dynamic Zero-Crossing Detector

- Not suitable as a general purpose comparator
  - Switching threshold depends on input waveform
- Fast
- Simple
- Rail-to-rail swing
- Amenable to scaling
- Energy efficient - draws no static current

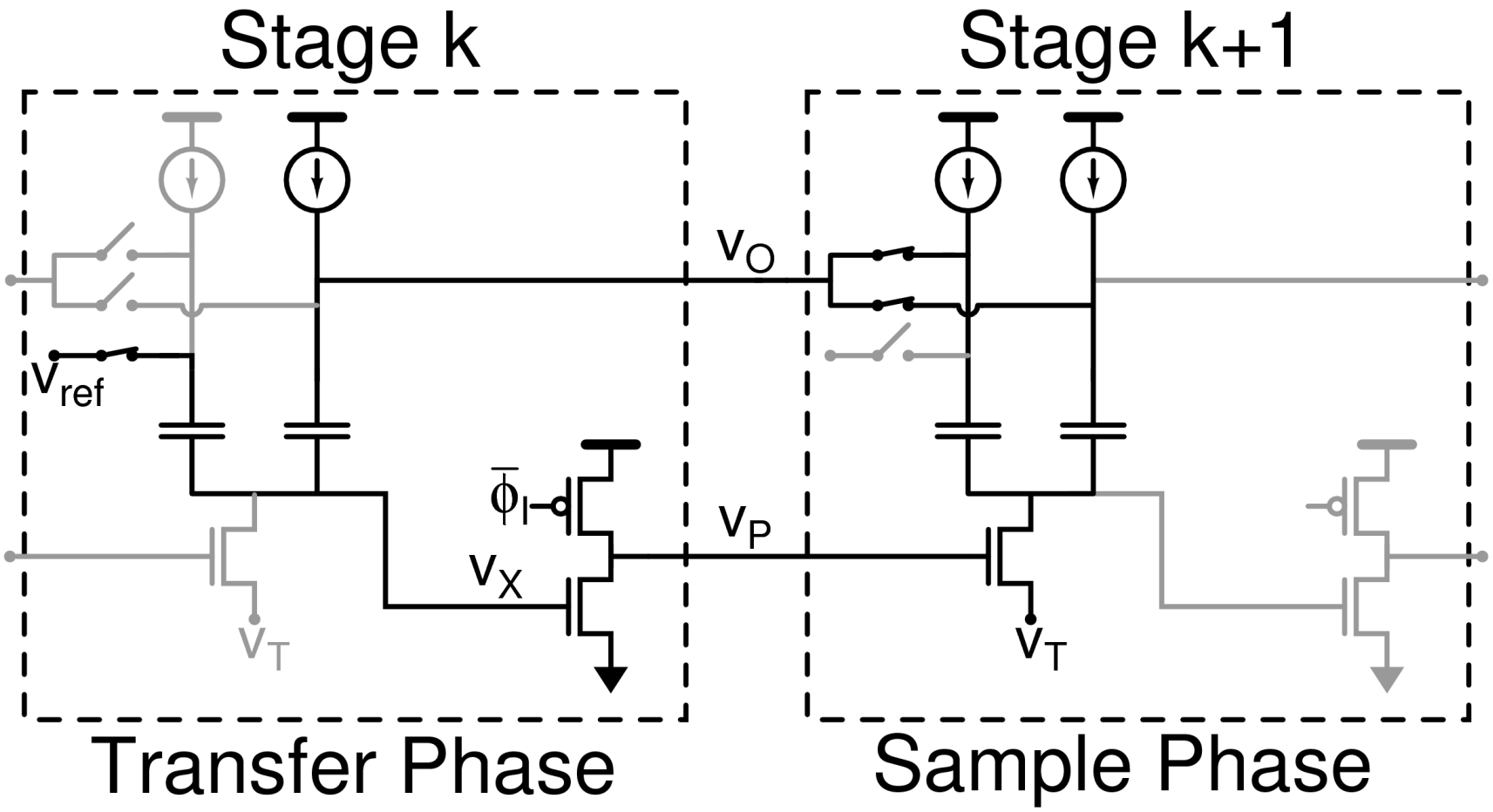


Dynamic Zero-Crossing Detector Limitations

- Inherently single-ended
  - Suitable for low to medium resolutions
- The offset is ramp-rate, temperature, and process dependent
  - An auto-zeroing circuit can null these dependencies



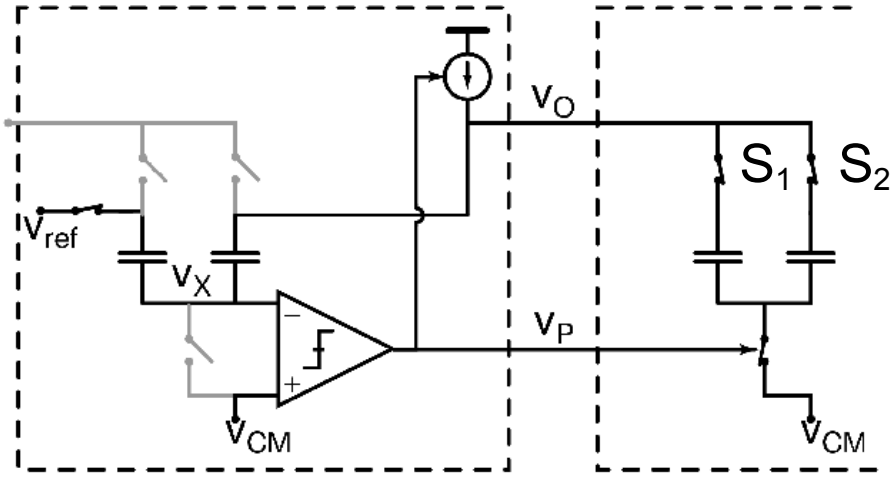
Simplified ZCBC Pipelined ADC Schematic



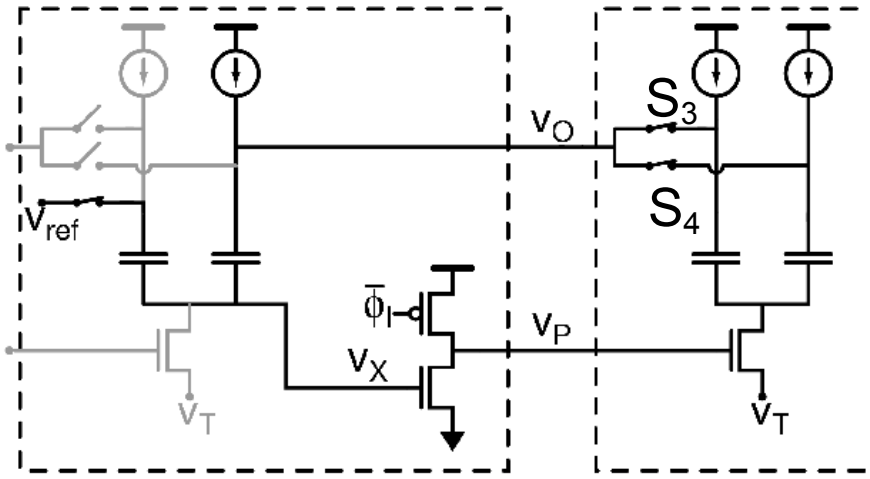
Current Source Splitting

- Switches S_1 and S_2 cause non-linearities and limits output swing
- Splitting the current source up removes the series switches
- Switches S_3 and S_4 remove current mismatch
- All other switches are connected to DC voltages and do not contribute non-linearities.

Original CBSC Schematic



This ZCBC Schematic

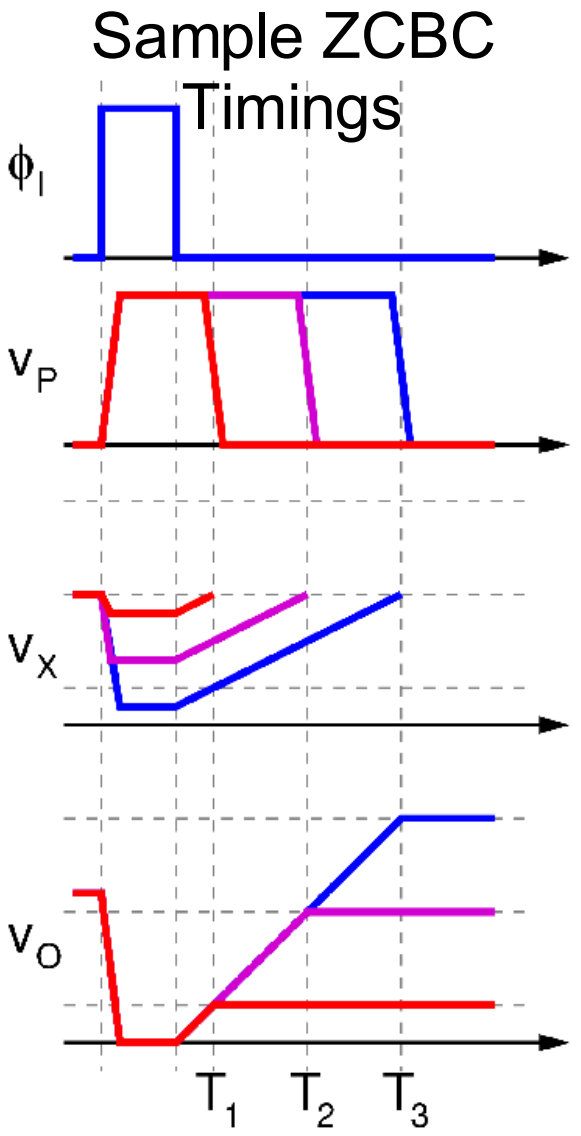


Bit Decision Comparators

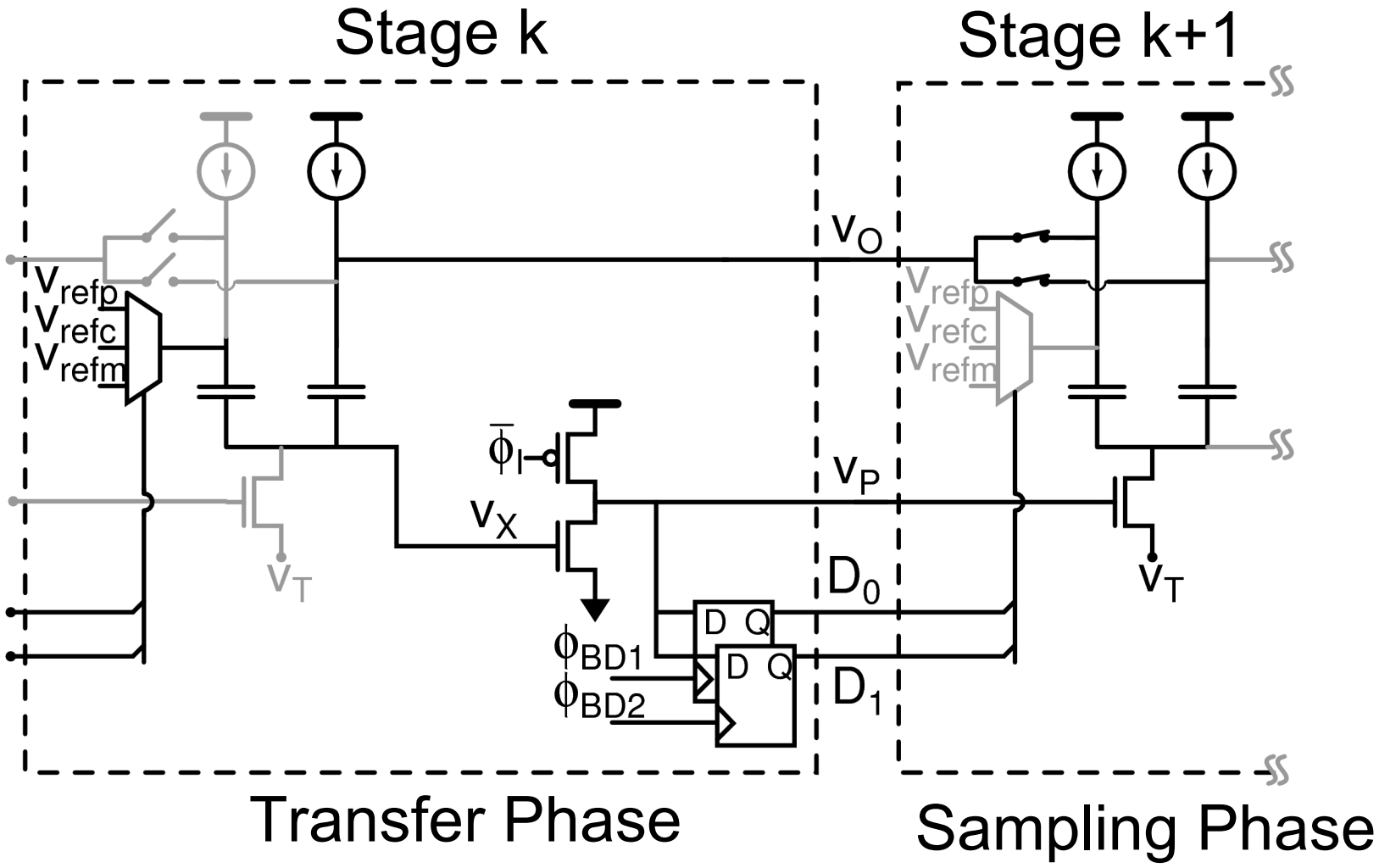
- Bit decisions comparators (BDC) provide a coarse quantization of the output voltage $\mathbf{v_o}$
- When implemented using clocked comparators, they lie in the critical path
  - They make their decision after one stage ends ramping and before the next stage can begin.
  - Meta-stability issues can arise if they are not given ample time to make their decision
  - Requires the design of a fast clocked comparator

Bit Decision Flip-Flops

- The time at which $\mathbf{v_P}$ switches is proportional to the output voltage.
- Sampling $\mathbf{v_P}$ with a **Bit Decision Flip-Flop** (BDFF) provides a coarse quantization.
- Analogous to a single-slope ADC.

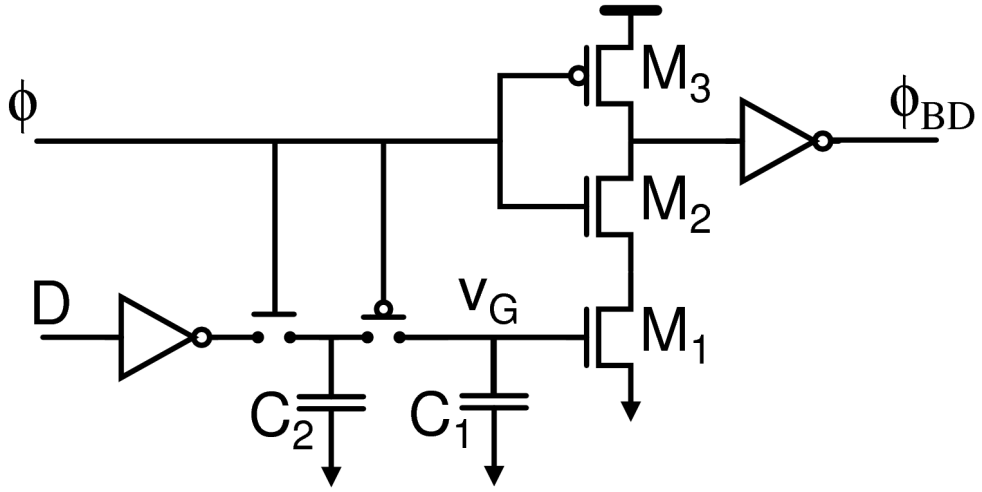


Complete ZCBC Schematic



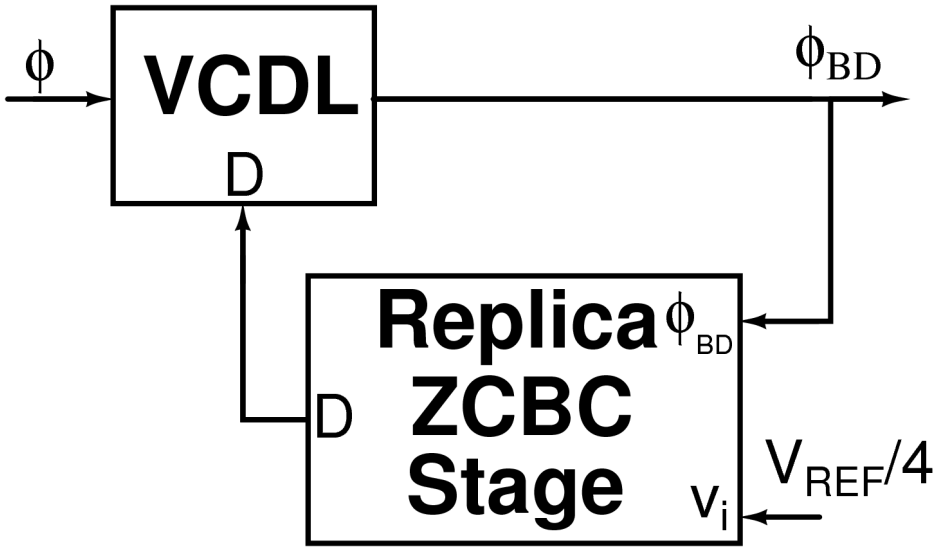
BDFF Phase Generation

- A Voltage Controlled Delay Line (VCDL) generates the bit decision clock phase
- A charge pump controls $\mathbf{v_G}$ to set the delay



BDFF Feedback Loop

- Use bit decision threshold $\mathbf{V_{REF}/4}$ as input into a replica ZCBC stage
- The bit decision **D** out of the replica stage indicates if ϕ_{BD} is ahead or behind
- **D** adjusts the VCDL delay each clock cycle
- The small amount of jitter on ϕ_{BD} in steady-state is not problematic because of over-range protection

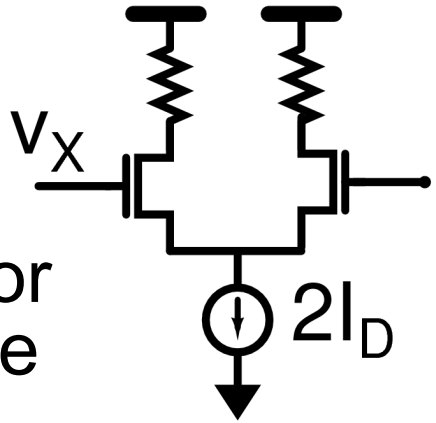


Bit Decision Flip-Flop Discussion

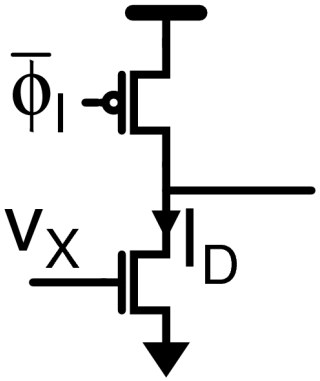
- Implementing the BDC as a flip-flop removes it from the critical path
  - The bit decisions are made in parallel with the voltage ramp and are ready by the time the transfer phase ends
  - Eliminates meta-stability issues
  - Eliminates the need for a fast clocked comparator
  - A standard flip-flop suffices
- A 1.5 bit/stage ADC requires 2 bit decision phases for $\pm V_{REF}/4$
  - A single ZCBC stage is switched between 2 VCDLs
- This method does not work for the 1st stage
  - Clocked comparators are used for the 1st stage

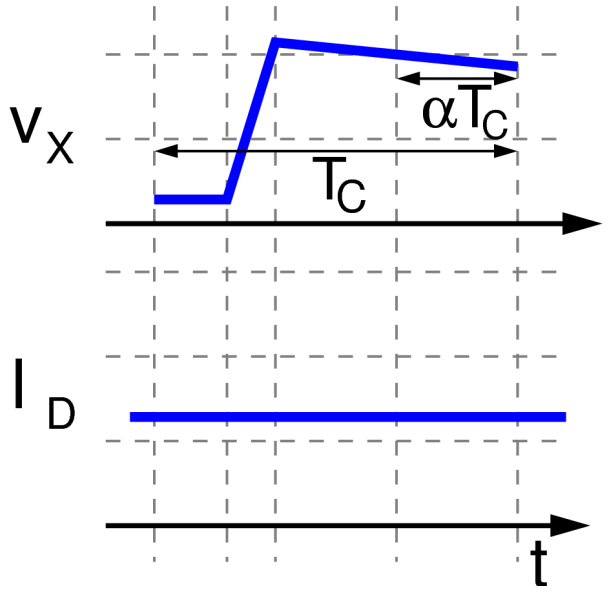
CBSC vs ZCBC

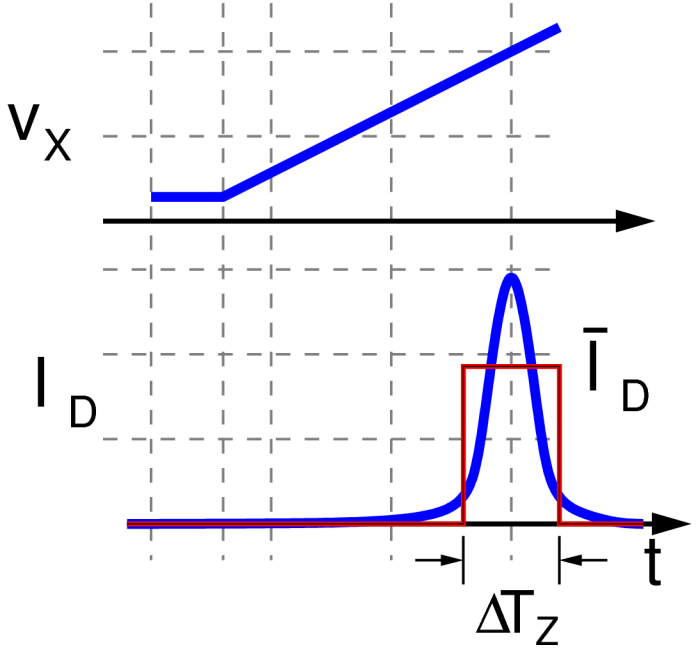
Original CBSC Comparator Input Stage



This ZCBC Zero-Crossing Detector







CBSC vs ZCBC

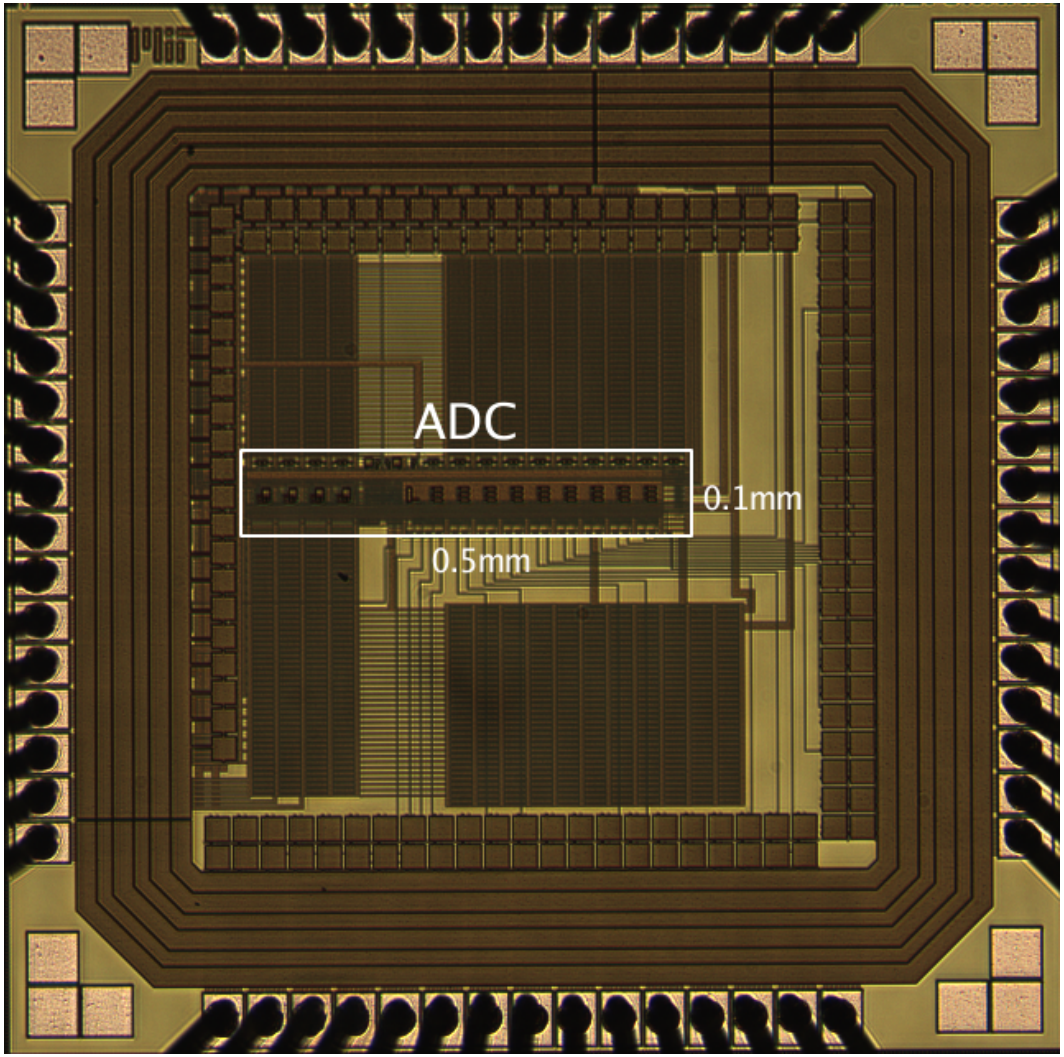
	Original CBSC[1]	This ZCBC
Energy	$2V_{DD}I_DT_C$	$V_{DD}\bar{I}_D\Delta T_Z$
Noise Bandwidth	$\frac{1}{2\alpha T_C}$	$\frac{1}{2\Delta T_Z}$
Noise Spectral Density	$\frac{8kT}{3I_D}(V_{GS}-V_T)$	$\frac{4kT}{3\bar{I}_D}(V_{GS}-V_T)$
Noise Energy Product $(\alpha = 0.5)$	$\frac{16}{3}kTV_{DD}(V_{GS}-V_T)$	$\frac{2}{3}kTV_{DD}(V_{GS}-V_T)$

- Theoretical 8x better performance from this ZCBC
  - This ZCBC only requires a single gain stage
  - Original CBSC can be fully differential

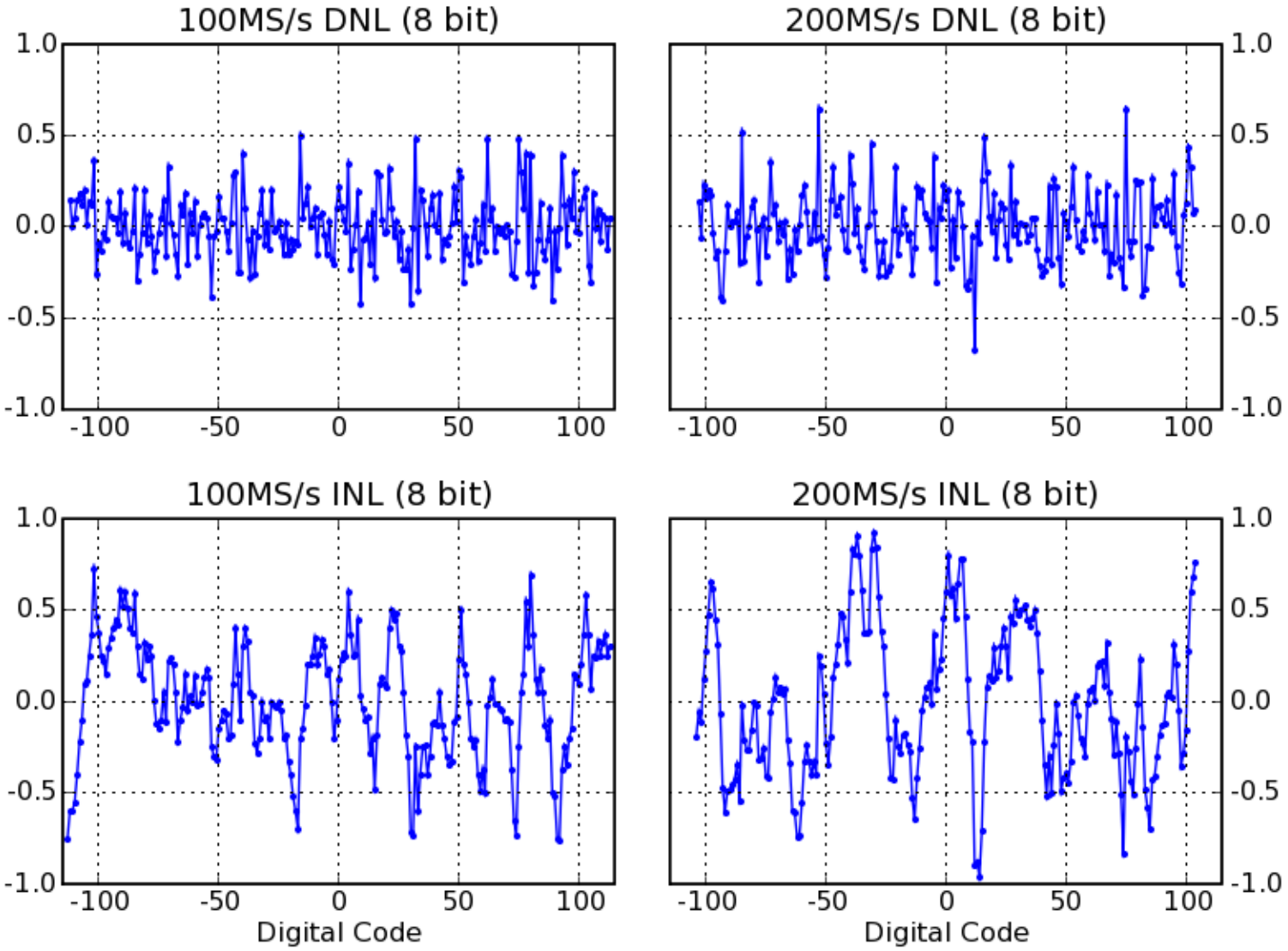
1. Forienza, et.al, JSSC, Dec 2006.

Chip Micrograph

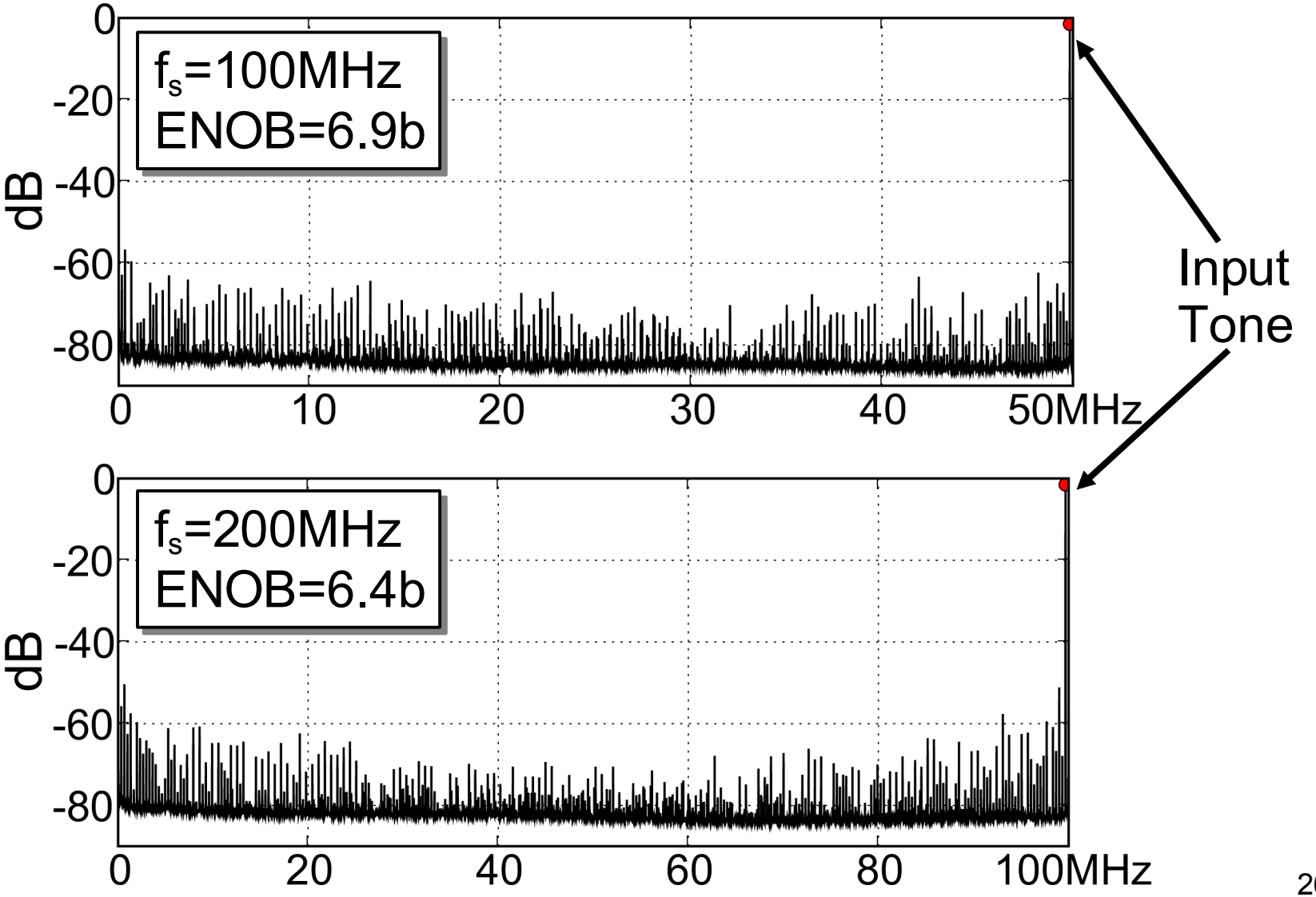
- 0.18um CMOS
- 0.05mm^2



Measured Results - Linearity

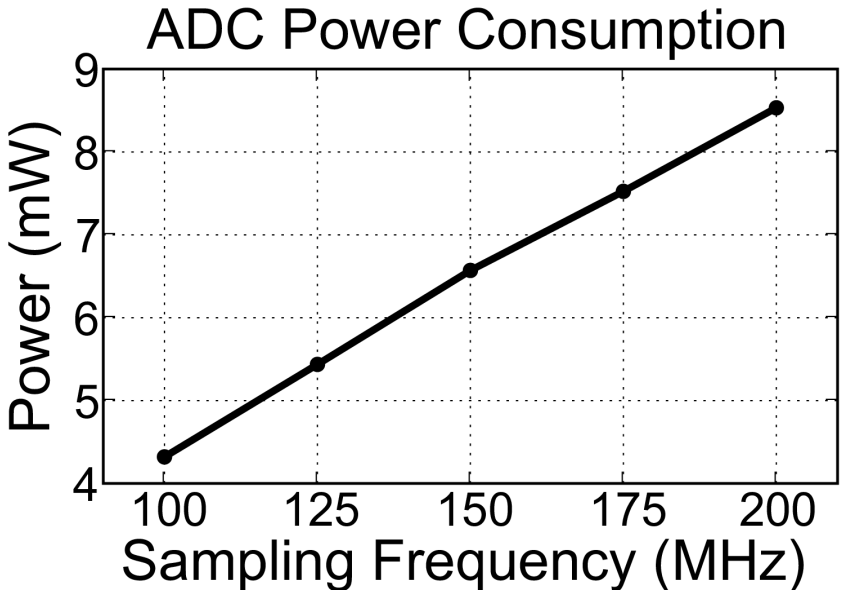


Measured Results – Frequency Response



Measured Results – Power Consumption

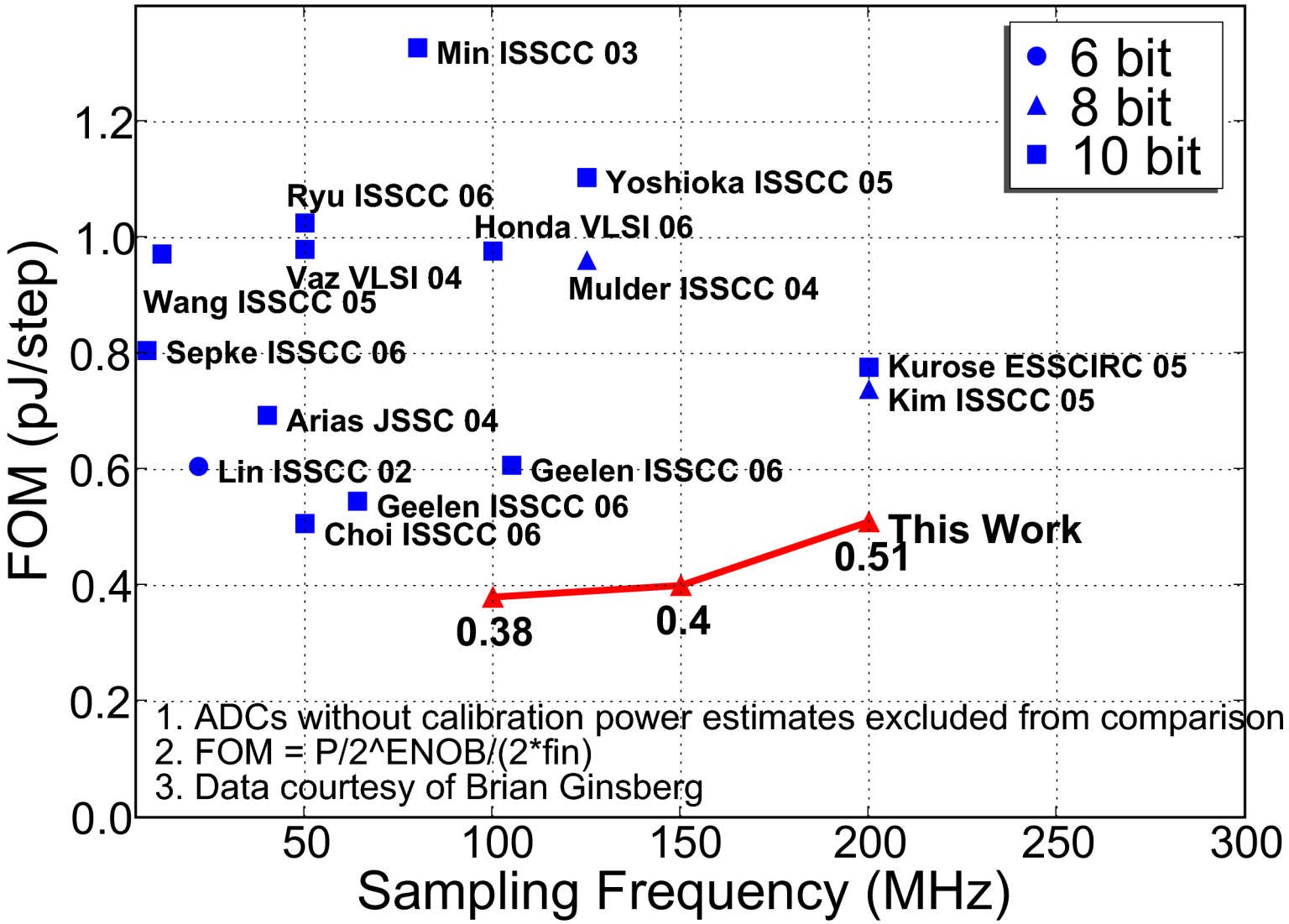
- The complete ADC draws NO static current.
  - The current sources provide the transfer charge only.
  - The DZCD consumes only the power necessary to switch the sampling switch.
- Only dynamic CV^2f power is consumed.



ADC Performance Summary

Sampling Freq.	100MHz	200MHz
Input Range	1V	1V
DNL	+/- 0.50 LSB	+/- 0.75 LSB
INL	+/- 0.75 LSB	+/- 1.00 LSB
ENOB	6.9b	6.4b
Power	4.5mW	8.5mW
FOM ($P/2^{ENOB}/2f_{in}$)	0.38 pJ/step	0.51 pJ/step

Measured Results – FOM Comparison



FOM Remarks

- 66% of the power consumption is from the digital power supply
  - Technology scaling will significantly improve the FOM
- The noise floor is more than 4x higher than theoretical and simulated results predict
  - Noise coupling from the I/O's is a problem
  - Deep NWELL, better packaging, etc. will help
  - Not all issues with this architecture are known
  - Work is underway to improve noise rejection and to reach theoretical performance.

Conclusions

- Introduced **Zero-Crossing Based Circuits** as a generalization of CBSC circuits
- Introduced an energy efficient **Dynamic Zero-Crossing Detector**
- Introduced **Current Source Splitting** to eliminate series switches and improve linearity
- Replaced clocked comparators with **Bit Decision Flip-Flops** to improve speed
- Demonstrated these techniques with an 8b, 200MS/s ZCBC Pipelined ADC

Acknowledgements

- MIT Center for Integrated Circuits and Systems (CICS) for funding
- National Defense Science and Engineering Graduate (NDSEG) Fellowship for funding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