9.3 A 12b 50MS/s Fully Differential Zero-Crossing-Based ADC Without CMFB

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As intrinsic device gain and power supply voltages decrease with CMOS technology scaling, it is becoming increasingly challenging for designers of conventional opamp-based switched-capacitor circuits to meet gain and output swing targets, and to ensure stability. Zero-crossing based circuits (ZCBC) are presented in [1-3] as an alternative architecture where each opamp is replaced with a current source and a zero-crossing detector. This changes the dynamics of the system while preserving the functionality. To further improve the robustness of ZCBC designs, we present a 50MS/s, 12b ZCBC pipelined ADC with fully differential signaling and automatic offset compensation.

A simplified schematic and timing diagram of 2 adjacent fully differential ZCBC pipeline stages are shown in Fig. 9.3.1 and Fig. 9.3.2, respectively. During the sampling phase, the input voltage is sampled onto sampling capacitors $C_{1\pm}$ and $C_{2\pm}$. The transfer phase begins when the pre-charge signal φ_{2I} turns on devices M_3, $M_{4\pm}$, and $M_{5\pm}$ to initialize the load capacitors $C_{3\pm}$ and $C_{4\pm}$ to V_{DD} and ground, respectively. This ensures that the differential output voltage starts below the minimum full-scale range. After the pre-charge phase, current sources $I_{2\pm}$, $I_{3\pm}$, and $I_{4\pm}$, which are split to avoid series switches for improved linearity [2], begin to charge the capacitors. The resulting voltage ramp continues until the zero-crossing detector (ZCD) detects the virtual ground condition, i.e. $v_{x+} = v_{x-}$. At this point, the ZCD output φ_{2e} turns off the differential sampling switch M_3 to sample the desired residue voltage.

In traditional opamp-based implementations, common-mode feedback (CMFB) is essential to keep both channels of the differential signal within range. CMFB is necessary because an opamp typically has common-mode gain. The common-mode gain of a ZCBC circuit, however, is relatively small and results from ramp rate differences between the positive and negative channels. The fully-differential ZCBC reported in [3] uses 2-phase charge transfer [1] and employs a conventional CMFB circuit during the coarse phase. In this work, single-phase operation is used for higher speed, making conventional CMFB circuitry difficult to implement. Therefore, the switching scheme shown in Fig. 9.3.1 and Fig. 9.3.2 is developed to remove the need for CMFB. In a conventional opamp-based implementation, switches $M_{4\pm}$ are left on for the entire transfer phase and the common-mode error is sampled onto the load capacitors. In this implementation, however, since these switches are turned on only during the pre-charge phase, the inside plates of the sampling capacitors are initialized to the common-mode voltage but are left to float when the output nodes ramp. The differential sampling switch (M_3) holds the inside plates together so they float at the same potential and ensures that C_{3+} and C_{4+} charge at the same rate as C_{3-} and C_{4-}. The parasitic capacitance on the inside plates holds the common-mode error, but the only effect is a small common-mode level shift at the input of the ZCD. Since the output common-mode is reset at the output of every stage by the preset operation, there is no stage-to-stage common-mode error accumulation. Thus, the low common-mode gain of the ZCBC combined with this alternative switching scheme enables the circuit to meet design specifications without any CMFB.

The schematic in Fig. 9.3.1 shows a power-supply feed-through asymmetry to the output nodes $v_{o\pm}$. Such an asymmetry limits the high-frequency power-supply noise-rejection capabilities of a fully differential circuit. To improve the power-supply noise rejection, symmetric dummy current sources (not shown in Fig. 9.3.1) that are permanently disabled are added on both the positive and negative channels to provide 1st-order parasitic capacitance matching between the power supplies and the output nodes. This ensures that high-frequency power-supply noise coupling is common-mode and does not get sampled on the differential output nodes $v_{o\pm}$.

The ZCD used in this design is shown in Fig. 9.3.3. A pre-amplifier consisting of differential pair devices M_1 and M_2 is actively loaded with a current mirror that performs a differential-to-single-ended conversion. The output of the pre-amplifier drives a dynamic threshold detector that is similar to the dynamic ZCD used in [2]. To save power, the output of the detector is also fed back to M_6 to turn off the bias current in the pre-amplifier as soon as the ZCD switches. The ZCD also features a digitally programmable offset. The schematic uses iterated-instance notation to succinctly draw parallel devices $M_3[3:0]$, $M_4[3:0]$, $M_a[3:0]$, and $M_b[3:0]$. Binary-weighted device widths in $M_3[3:0]$ and $M_4[3:0]$ can be enabled with devices $M_a[3:0]$ and $M_b[3:0]$ to modify the current gain of the current mirror and provide a digitally programmable offset to the ZCD.

Offset in a ZCBC design comes from conventional sources such as device mismatch as well as the voltage ramp overshoot due to the finite delay of the ZCD. In this work both sources of error are removed by a chopping technique similar to [4] and depicted in the block diagram of Fig. 9.3.4. The input signal is modulated with the chopping signal φ_c. The ADC converts the modulated signal, and then prior to demodulation, a Chopper Offset Estimator (COE) uses the digital output of the ADC to estimate the offset. The Offset Controller (OC) adjusts the digitally programmable offset of the ZCD in each stage to null the offset in the analog domain. The COE works by computing the mean of the signal over a block of data. The OC looks at the sign of the mean and drives an up/down counter to adjust one side of the current mirror in the ZCD.

This ADC employs redundancy that samples the input voltage on all MDAC and feedback capacitors [5] to reduce the ZCD noise referred to the ADC input rather than improve the closed-loop bandwidth. Additional redundancy is further used to reduce the required output voltage range. This is implemented by using a 3.3b sub-ADC in each 4× gain MDAC, increasing the reference voltages to be larger than the input voltage range, and placing the bit decision boundaries appropriately (see the block diagram and residue plot of Fig. 9.3.4). This improved effective output range gives more headroom to the current sources for improved linearity.

Implemented in $0.3mm^2$ in a 90nm CMOS process with a power supply voltage of 1.2V, this design consumes 4.5mW at 50MS/s. The DNL, INL and frequency response are shown in Fig. 9.3.5. The DNL is within ±0.5 LSB and the INL is within ±3 LSB on a 12b scale. The SNDR and SFDR are 62dB and 68dB, respectively. The noise floor is 72.3dB below full scale, showing that this design is distortion-limited. The dominant source of distortion comes from offsets in the bit-decision comparators that make up the sub-ADC of each stage. These offsets are larger than Monte-Carlo simulation predicted and cause the cascoded current sources to leave saturation when the residue nears the positive reference. The measured ENOB to a near-Nyquist-rate input tone is 10.0b and 10.6b at 50MS/s and 25MS/s, respectively, and the resulting FOM is 88fJ/conversion-step and 98fJ/conversion-step. The die micrograph is shown in Fig. 9.3.7.

References:
[1] J. Fiorenza et. al., "Comparator-Based Switched-Capacitor Circuits for Scaled CMOS Technologies," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2658-2668, Dec. 2006.
[2] L. Brooks and H.-S. Lee, "A Zero-Crossing Based 8-bit 200MS/s Pipelined ADC," *IEEE J. Solid-State Circuits*, vol. 42, no. 12, pp. 2677-2687, Dec. 2007.
[3] S.-K. Shin et. al., "A Fully-Differential Zero-Crossing-Based 1.2V 10b 26MS/s Pipelined ADC in 65nm CMOS, " *IEEE Symp. VLSI Circuits*, pp. 218-219, June 2008.
[4] H. van der Ploeg et.al., "A 2.5-V 12-b 54-MSample/s 0.25-μm CMOS ADC in 1-mm² with Mixed-Signal Chopping and Calibration," *IEEE J. Solid-State Circuits*, vol. 36, no. 12, pp. 1859-1867, Dec. 2001.
[5] S. Lewis et.al., "A 10-b 20-MSample/s Analog-to-Digital Converter," *IEEE J. Solid-State Circuits*, vol. 27, no. 3, pp. 351-358, Mar. 1992.
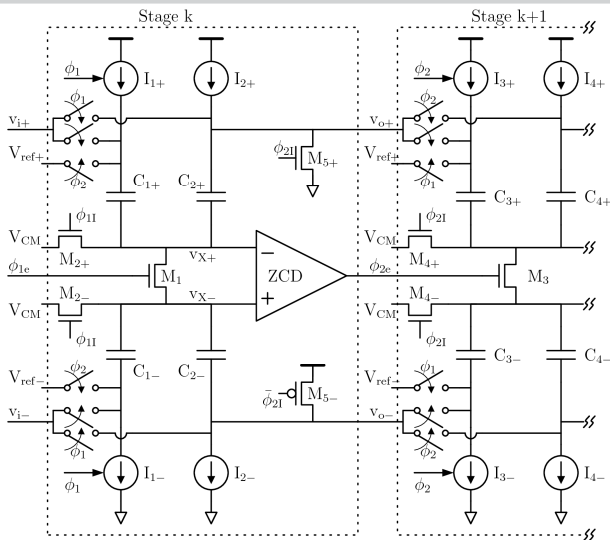
Stage k Stage k+1

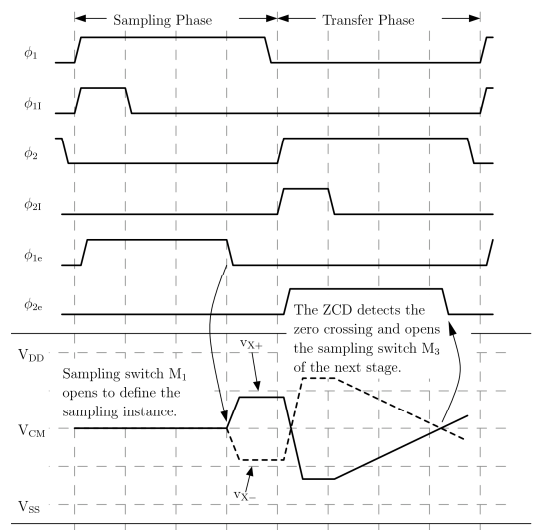Figure 9.3.1: Simplified schematic of 2 stages of a fully differential ZCBC pipelined ADC.

Sampling Phase Transfer Phase

The ZCD detects the zero crossing and opens the sampling switch M_3 of the next stage.

Sampling switch M_1 opens to define the sampling instance.

Figure 9.3.2: Timing diagram for ZCBC pipelined ADC.

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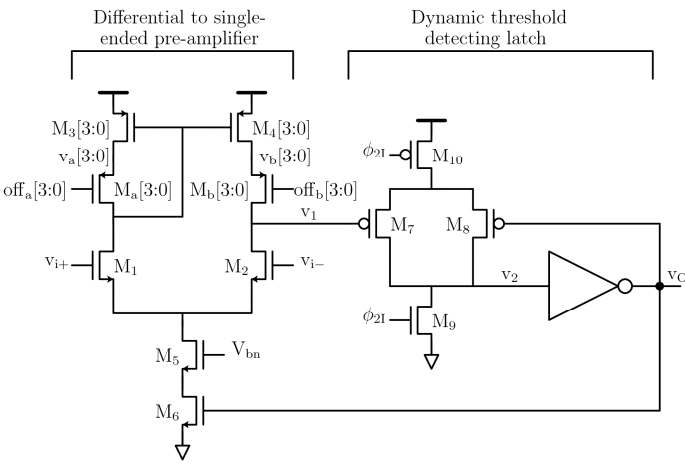Differential to single-ended pre-amplifier   Dynamic threshold detecting latch

Figure 9.3.3: Zero-Crossing Detector (ZCD) used in this design featuring digital offset programmability.

Residue Plot
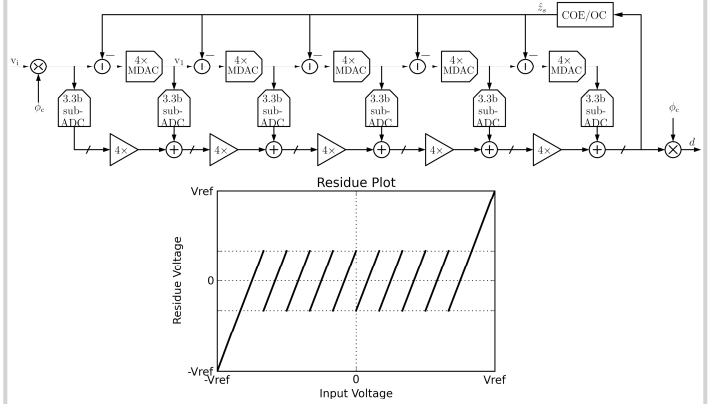
Figure 9.3.4: Pipelined ADC showing systematic offset cancellation technique via chopper offset estimation.
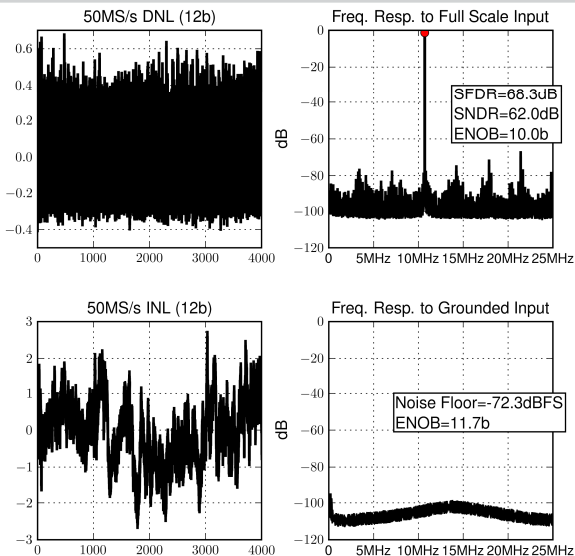
50MS/s DNL (12b)

Freq. Resp. to Full Scale Input

SFDR=68.3uB
SNDR=62.0dB
ENOB=10.0b

50MS/s INL (12b)

Freq. Resp. to Grounded Input

Noise Floor=-72.3dBFS
ENOB=11.7b

Figure 9.3.5: Measured DNL, INL, and frequency responses.

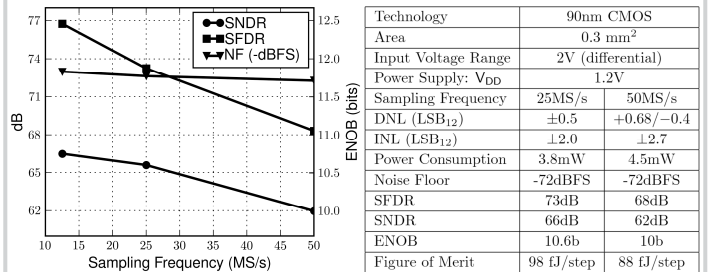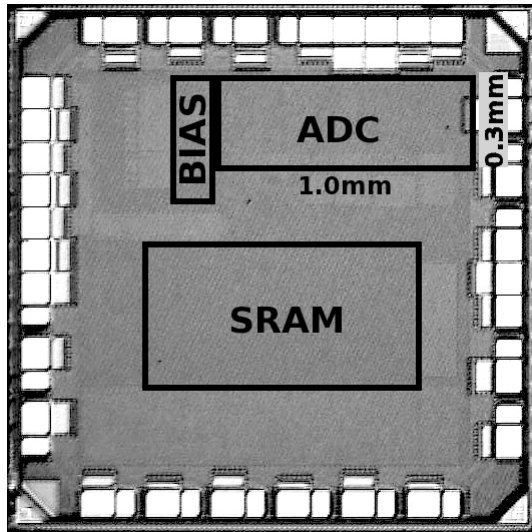| Technology	90nm CMOS	
Area	0.3 mm^2	
Input Voltage Range	2V (differential)	
Power Supply: V_{DD}	1.2V	
Sampling Frequency	25MS/s	50MS/s
DNL (LSB$_{12}$)	±0.5	+0.68/−0.4
INL (LSB$_{12}$)	⊥2.0	⊥2.7
Power Consumption	3.8mW	4.5mW
Noise Floor	-72dBFS	-72dBFS
SFDR	73dB	68dB
SNDR	66dB	62dB
ENOB	10.6b	10b
Figure of Merit	98 fJ/step	88 fJ/step

Figure 9.3.6: Summary of measured performance.

Figure 9.3.7: Die micrograph.