9.3 A 12b, 50MS/s Fully Differential Zero-Crossing Based ADC Without CMFB

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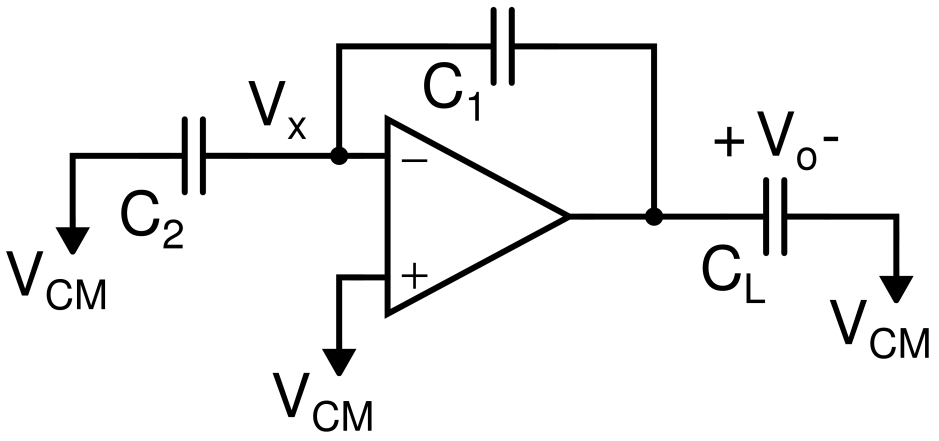
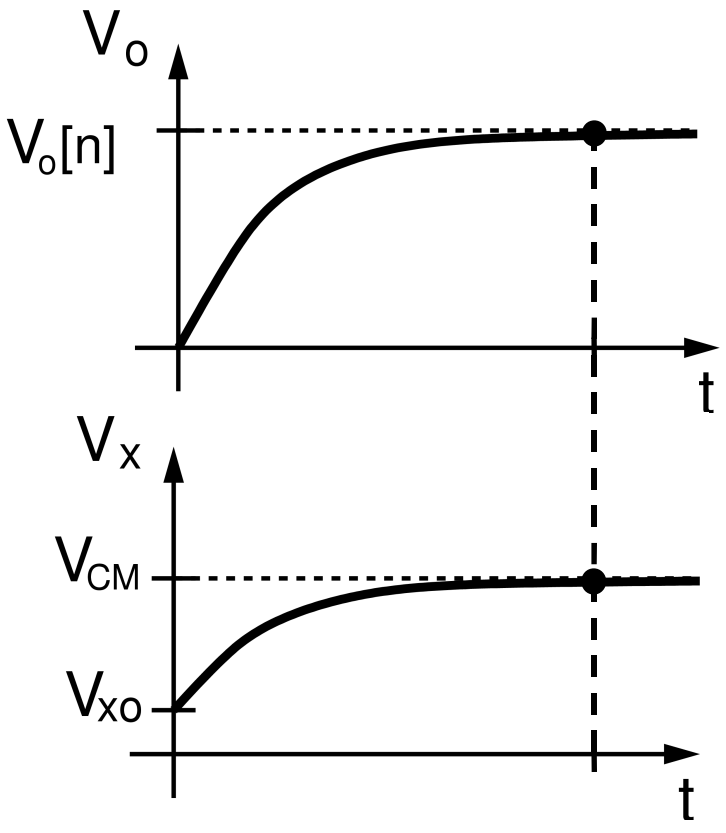
Outline

- Review of zero-crossing based circuits
- Fully-differential implementation
- Common-mode control
- Chopper offset estimation
- Reference voltage switching
- Output range enhancement
- Results
- Conclusion

Op-amp Based Transfer Phase

- **Op-amp forces virtual ground condition**
- **Exponential settling to virtual ground**



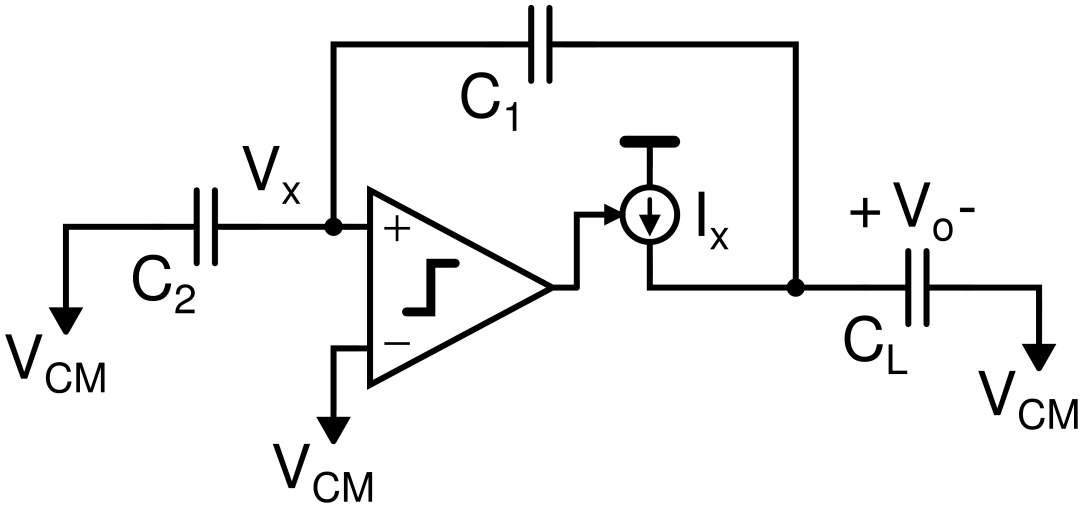


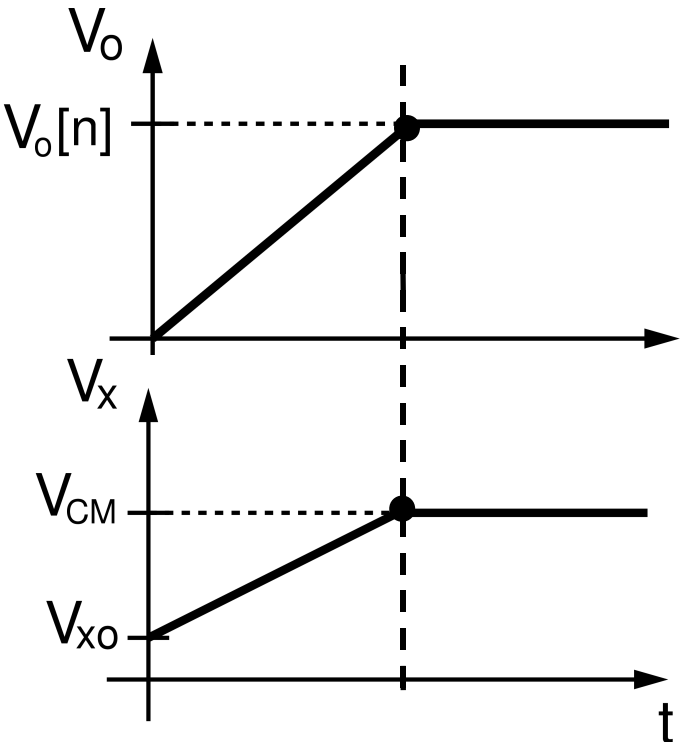
Op-amp Based Circuit Issues

- **Op-amp must provide high gain and reasonable output swing simultaneously.**
  - **Difficult to achieve in scaled CMOS**
  - **Requires cascading, gain enhancement, etc.**
  - **Added devices contribute noise**
- **Op-amp must be stable under feedback.**
  - **High gain requirement conflicts with stability**
- **Fast, high accuracy settling requires high bandwidth, thus large noise bandwidth.**
- **The combined result is high power consumption.**

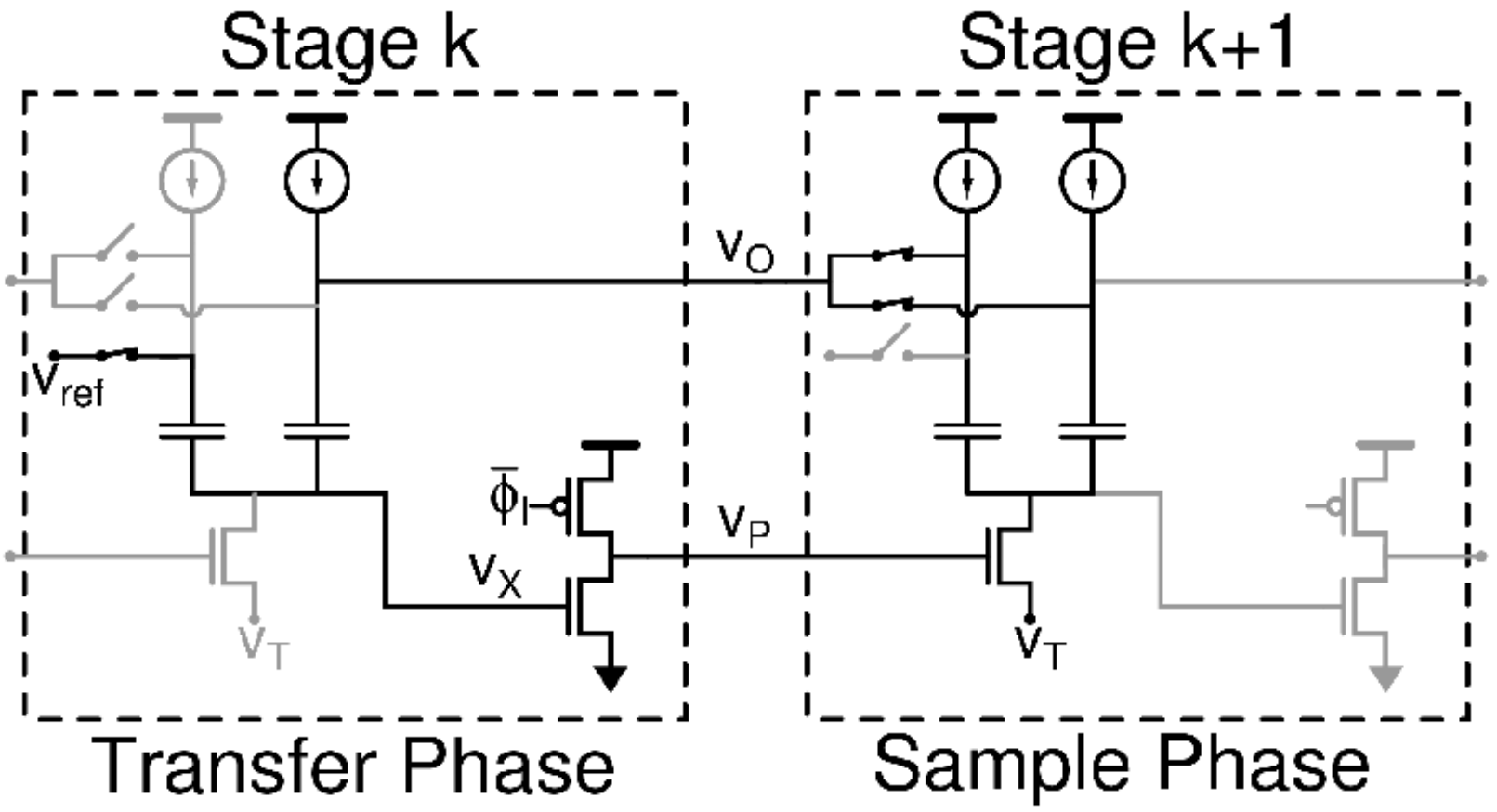
Zero-Crossing Based Circuits (ZCBCs)

- **Current source sweeps the output voltage**
- **Zero-Crossing Detector (ZCD) detects virtual ground condition and turns off current source**
- **Same output voltage is obtained**
- **Sub kT/C noise**





Previous ZCBC Pipelined ADC

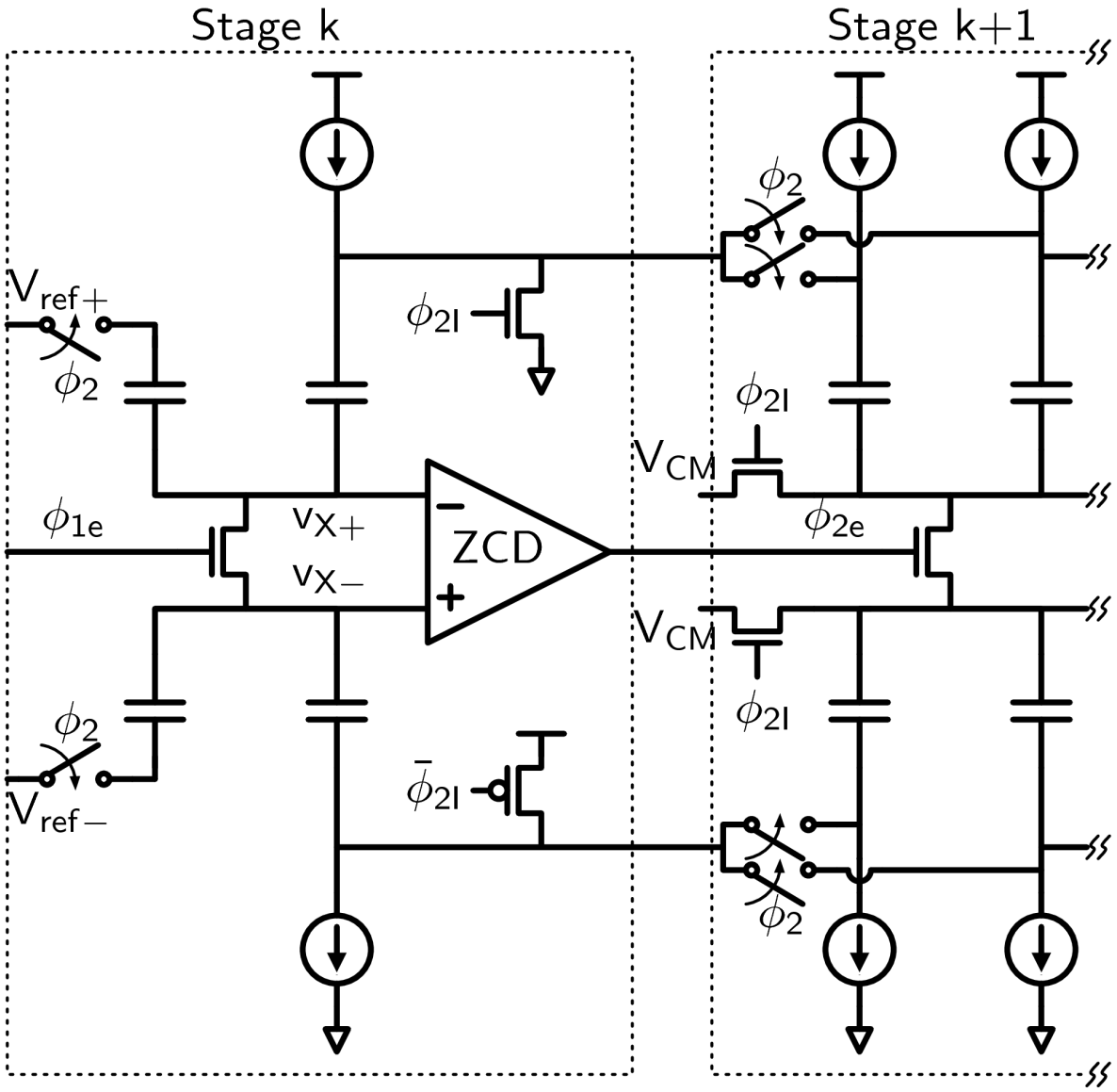


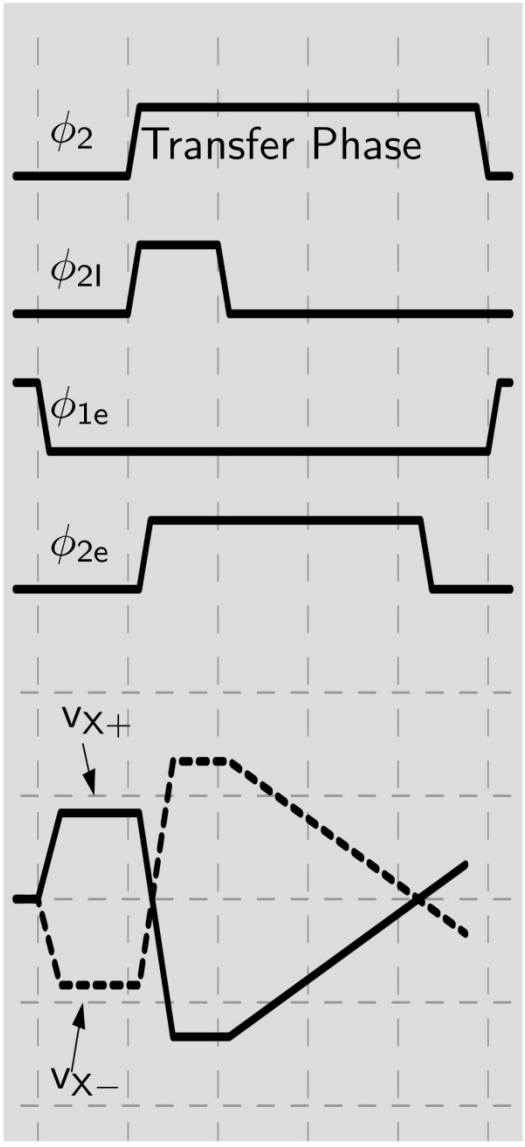
- **Brooks & Lee, "A Zero-Crossing Based 8b, 200MS/s Pipelined ADC", ISSCC, Feb 2007.**

Single-Ended Implementation

- **Advantages**
  - **Simple and fast**
  - **ZCD consumes only CV^2f power**
- **Issues**
  - **Noise rejection: I/O noise caused 8x higher floor than predicted**
  - **Offset compensation was not implemented**

Fully Differential Schematics

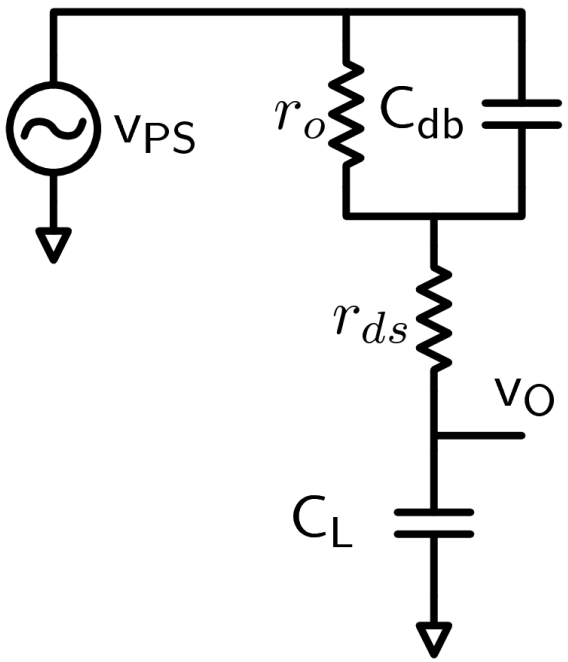


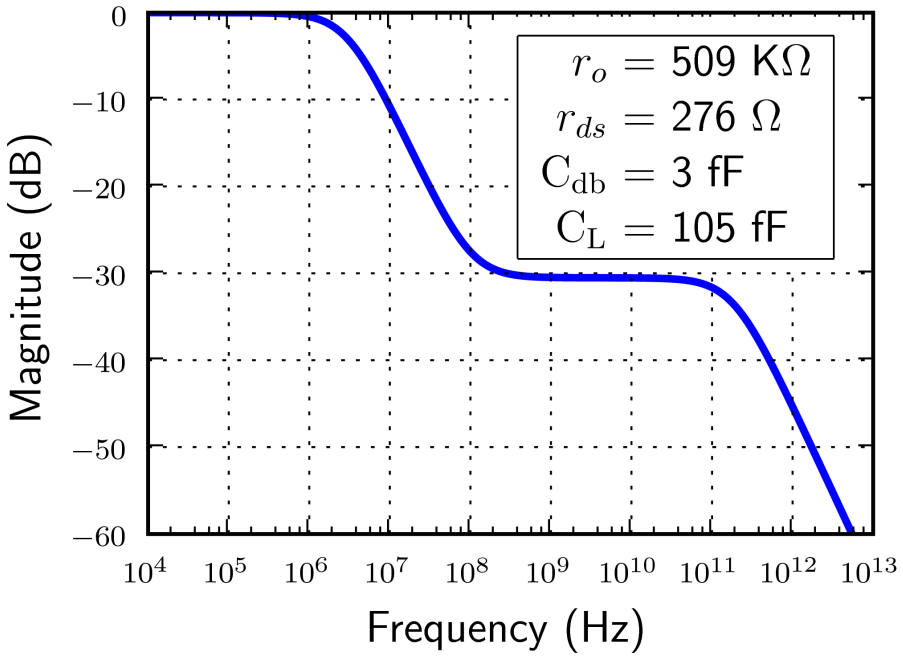


Common-Mode Control

- **Op-amp based implementations:**
  - **Typically have large common-mode gain**
  - **Require common-mode feedback**
- **Zero-crossing based implementations:**
  - **Common-mode is reset at the output of each stage**
  - **Small common mode variation caused by current source mismatch**
  - **Common-mode feedback is unnecessary**

Power Supply Noise



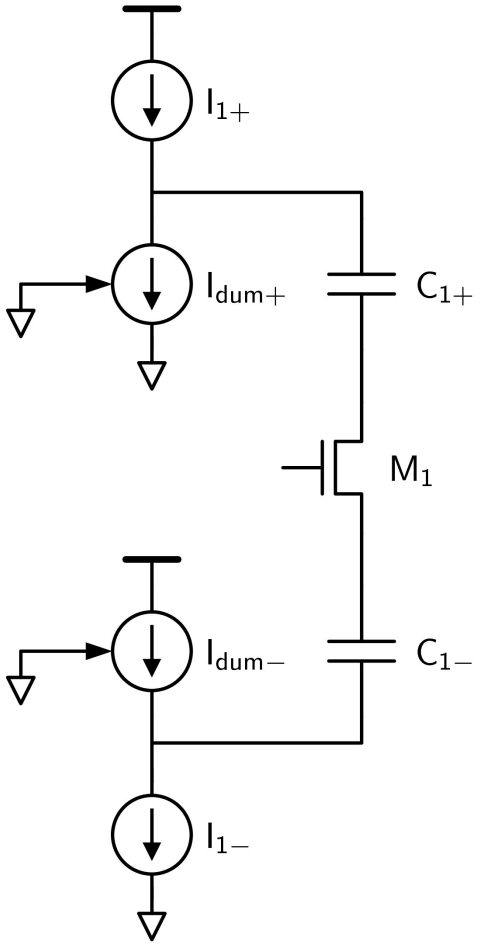


$$\frac{v_O(s)}{v_{PS}(s)} \approx \frac{sr_oC_{db}+1}{(sr_oC_L+1)(sr_{ds}C_{db}+1)}$$

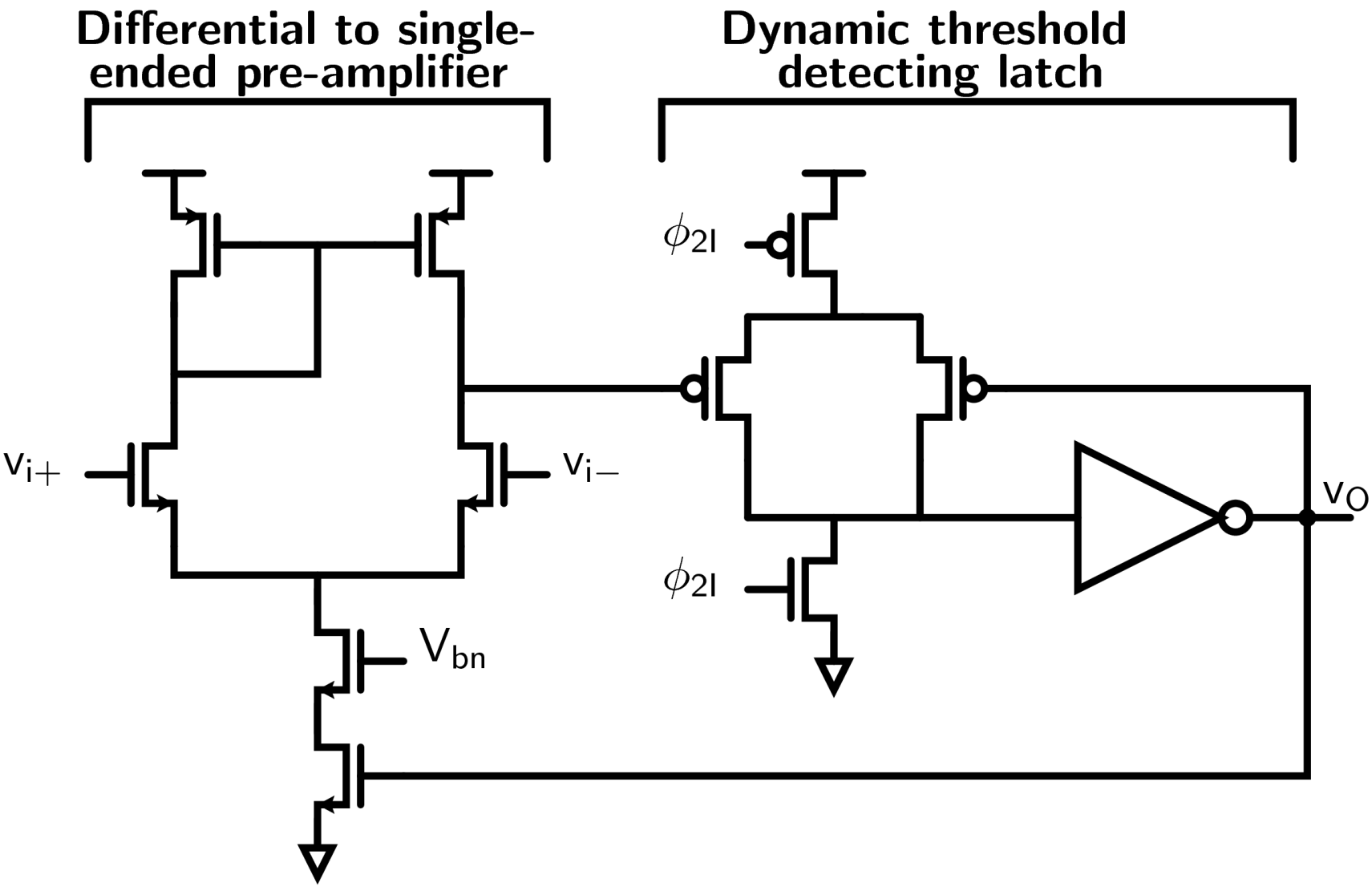
- **ZCD tracks & nulls low frequency supply noise**
- **High frequency noise feeds to the output node**

Replica Dummy Current Sources

- **Replica current sources added for symmetry**
- **Dummy current sources are always off**
- **Creates matching parasitics on output nodes**
- **High frequency noise couples symmetrically**



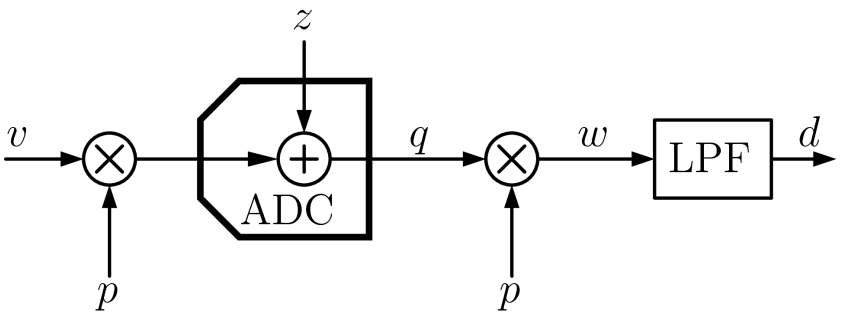
Differential ZCD



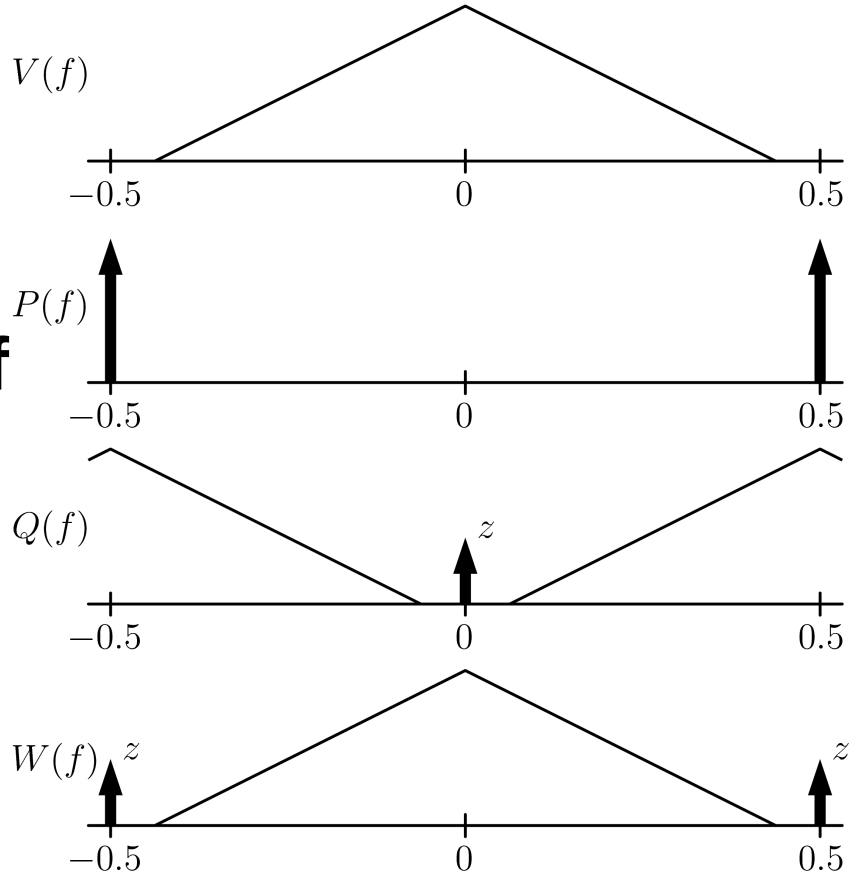
Offset Compensation

- **ZCBC is not compatible with traditional closed loop offset sampling**
- **Closed loop offset compensation doubles power consumption and noise**
- **Chopper Offset Estimation (COE) was developed for this design**

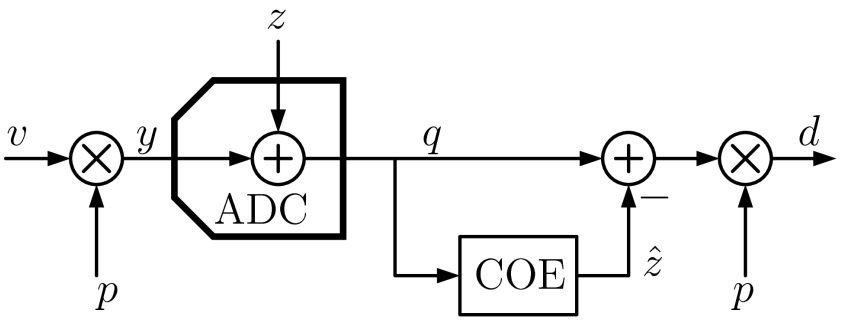
Traditional Chopper Stabilization



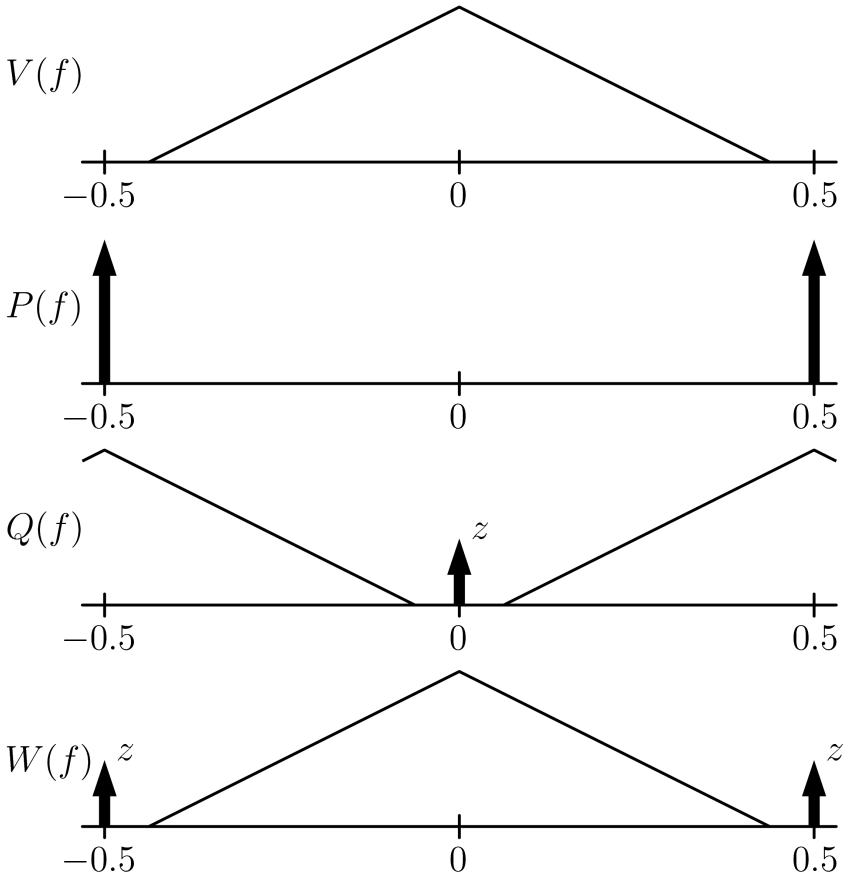
- **Offset is modulated out of band**
- **Output is digitally demodulated**
- **Low-pass filter removes offset**



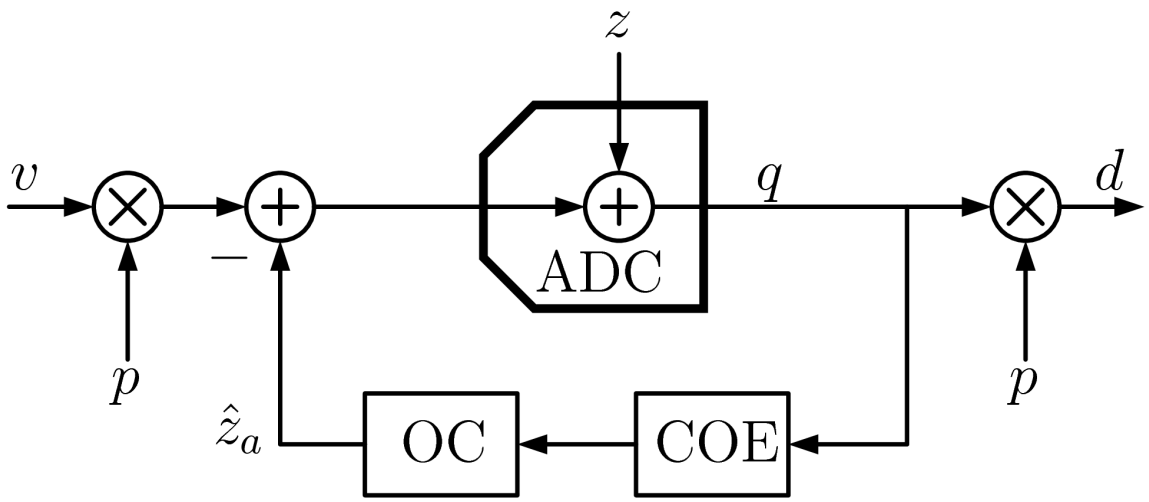
Chopper Offset Estimation



- **COE is narrow band LPF**
- **Poly-phase decomposition of COE realizes significant hardware savings**

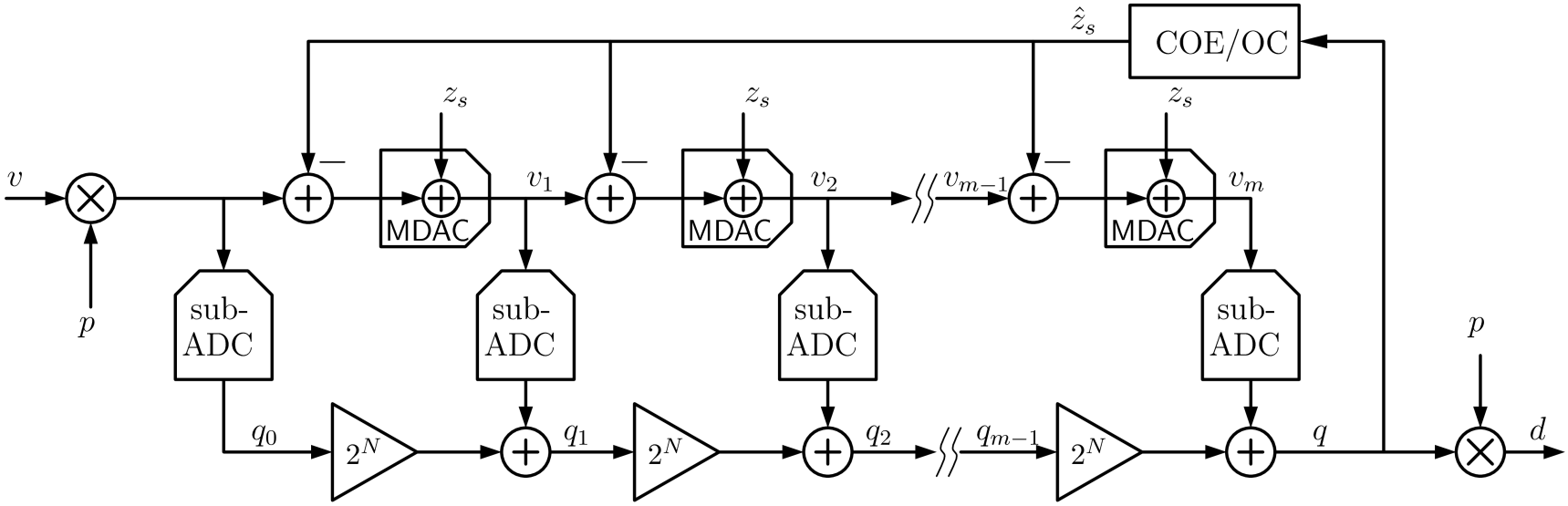


Input Referred COE



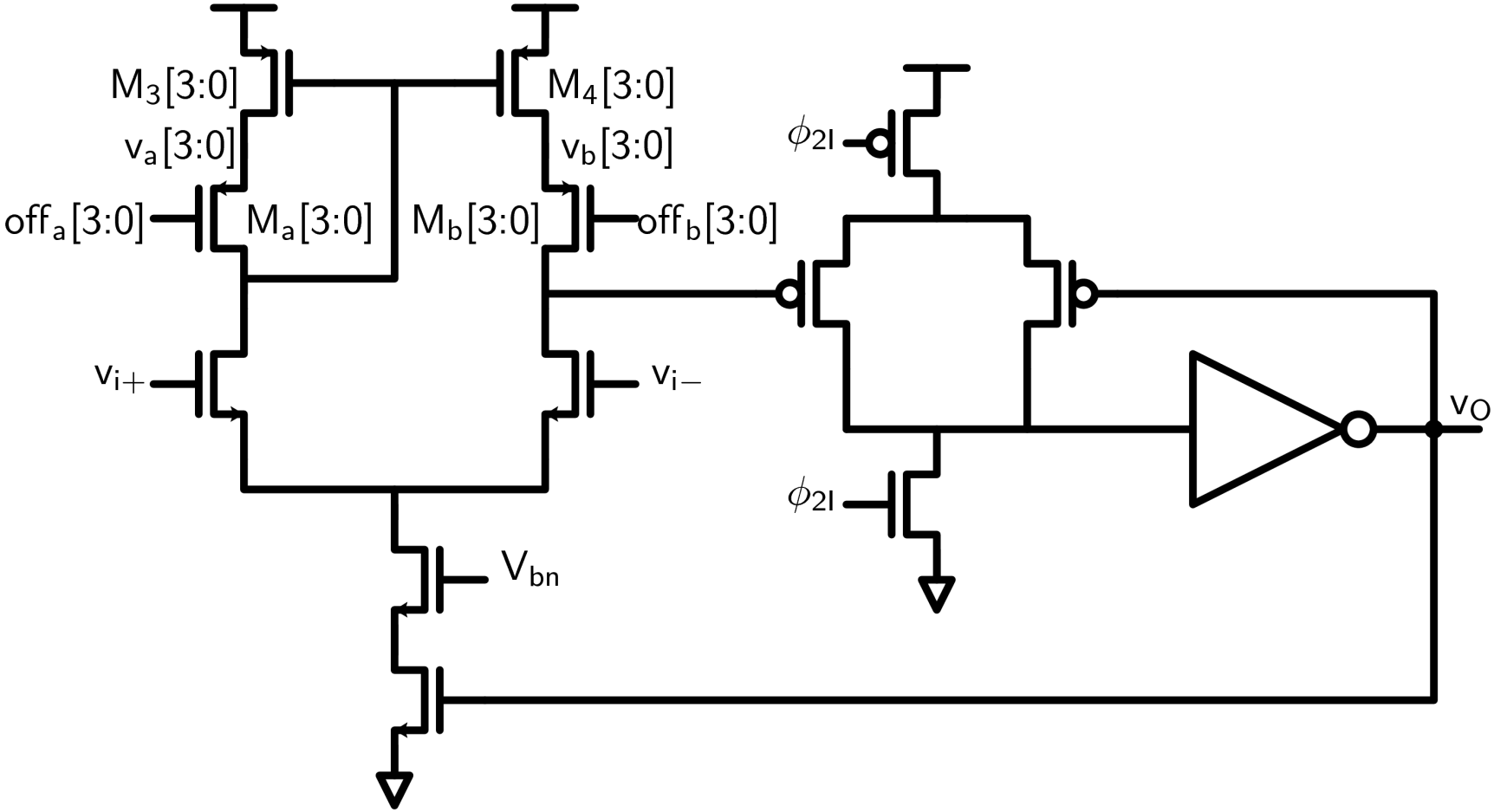
- **Offset estimate fed back into analog domain**
- **Nulls offset at the source to recover lost signal range**
- **Offset Controller (OC) converts measured digital offset to analog nulling factor**

COE for Pipelined ADCs



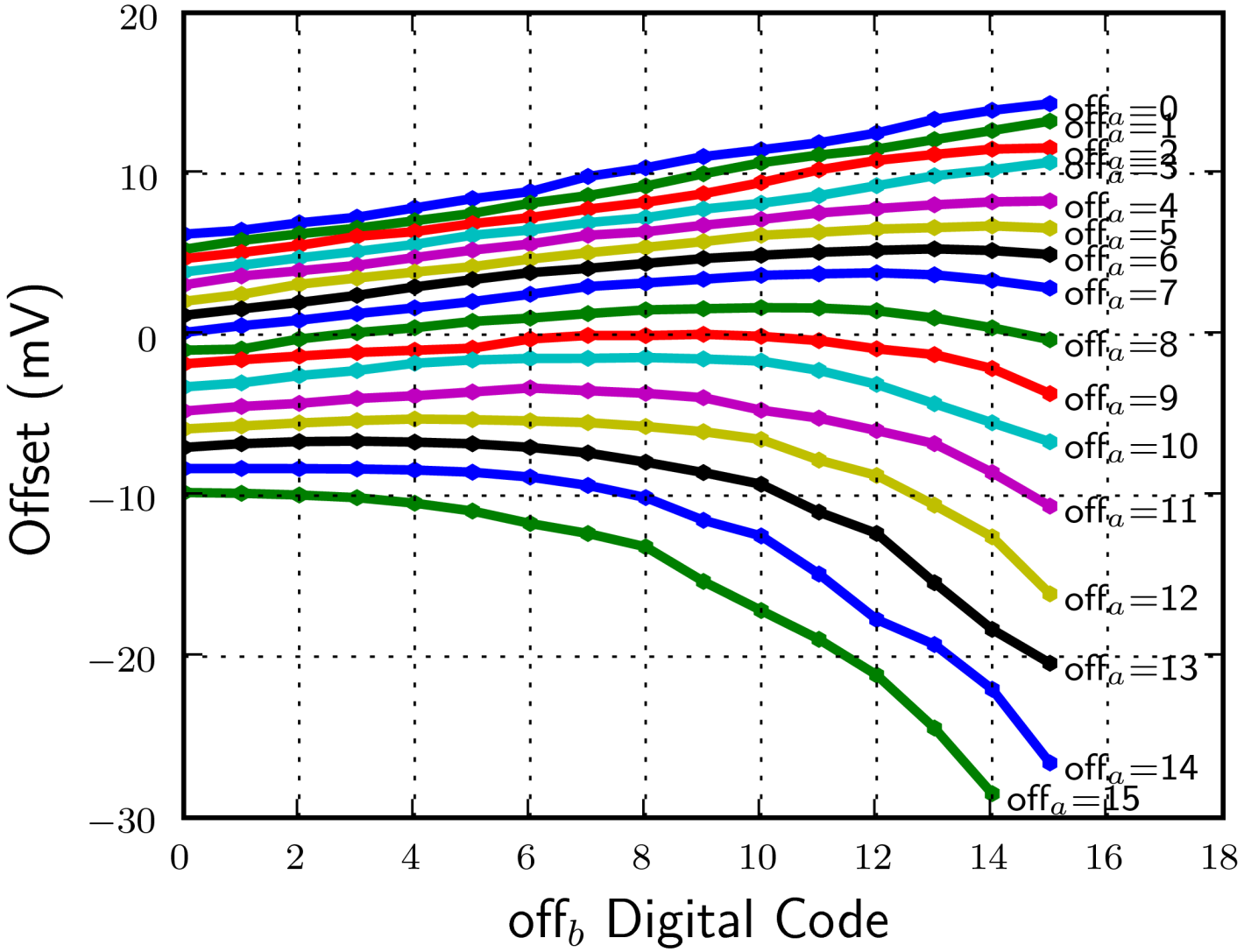
- **Systematic offset due to overshoot is nulled at each stage with single controller**
- **Also removes random offset due to mismatch**

ZCD With Offset Compensation

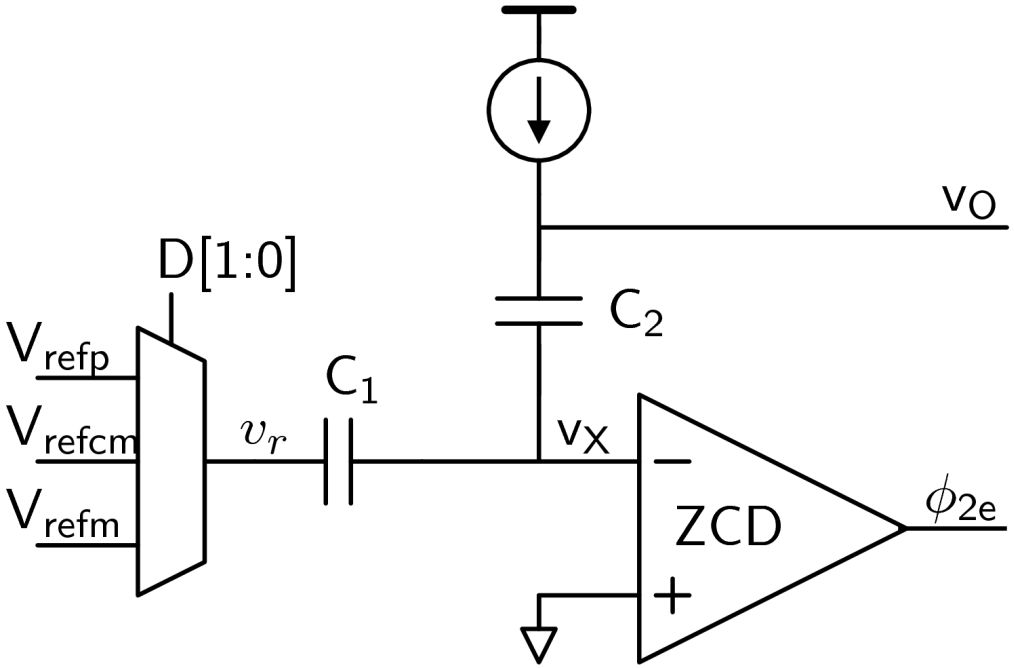


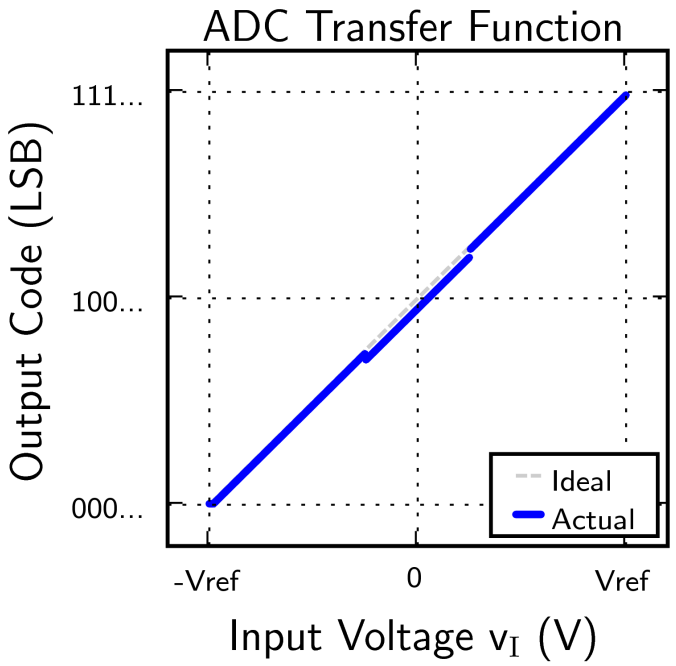
- **Switches create programmable current gain mirror**
- **Provides power efficient digital offset adjustment**

Measured ZCD Offset Range



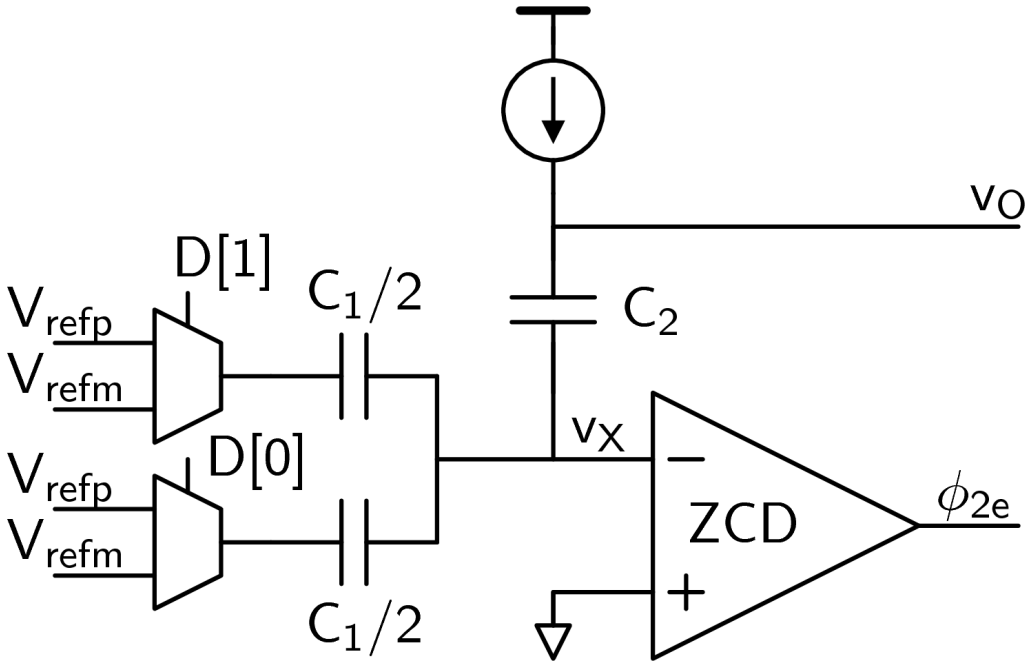
Reference Switching Issue





- **1.5b/stage example**
- **Different voltage drops across reference voltage switches cause DNL**

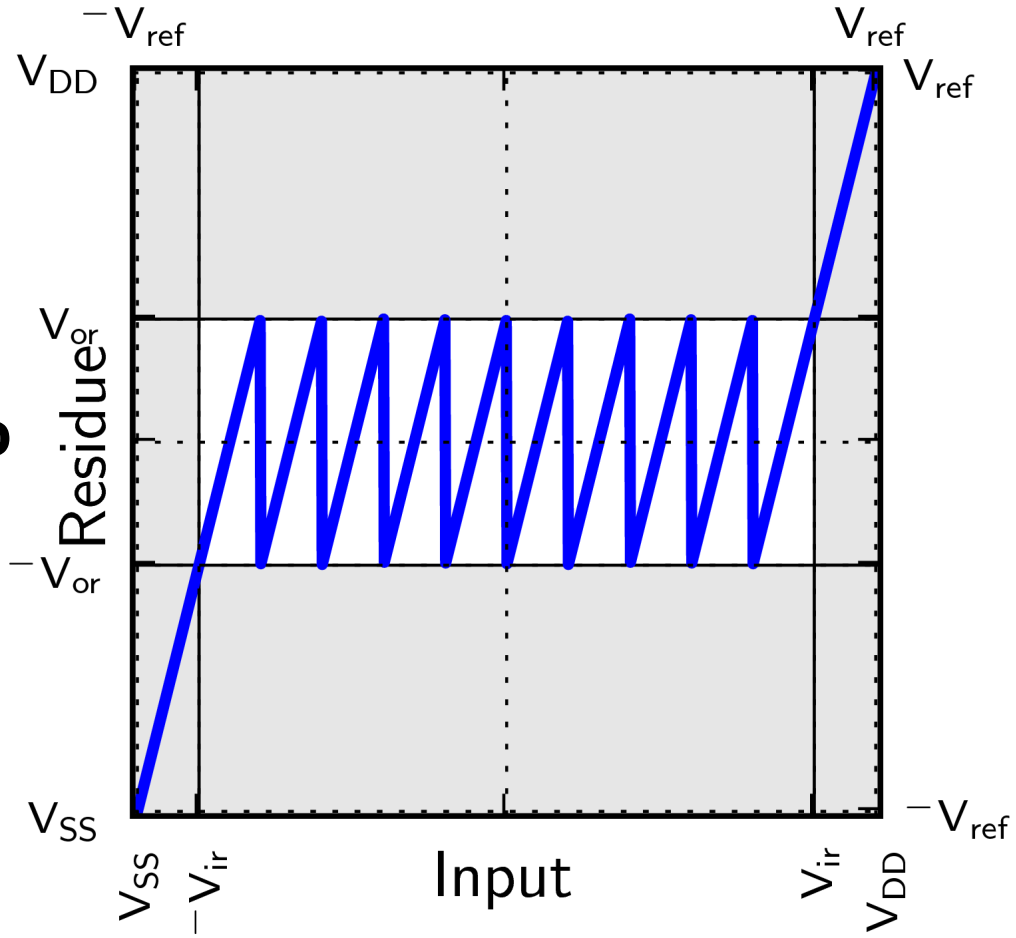
Alternative Switching Scheme



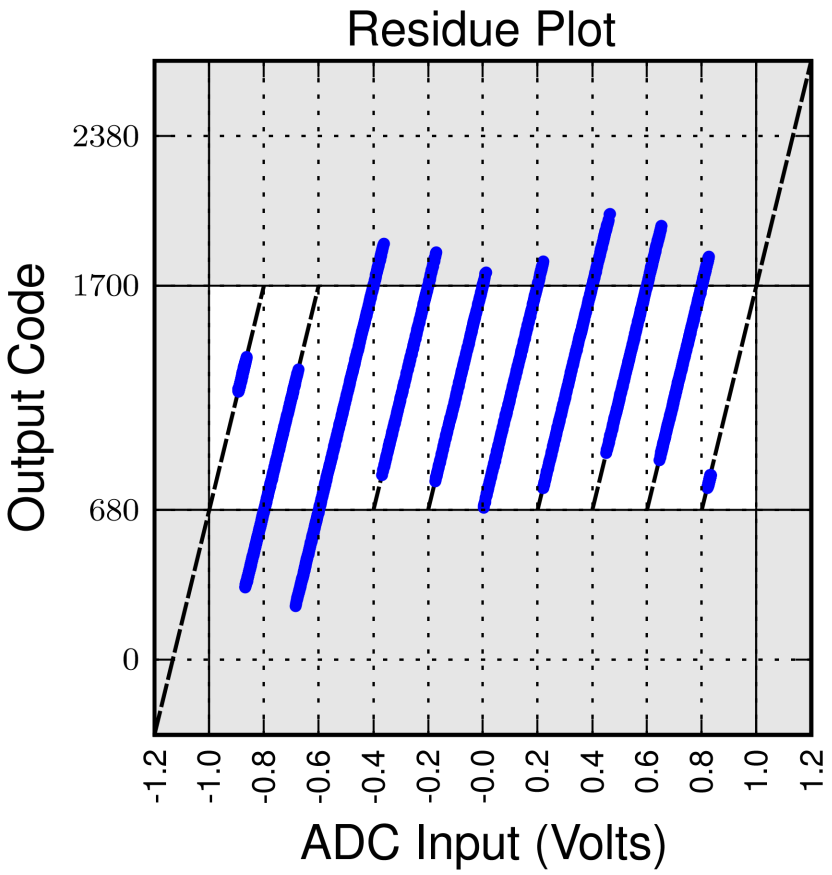
- **Splitting C_1 and driving differentially eliminates middle voltage V_{refc}**
- **Voltage drop no longer creates non-linearity**
- **Leaves bit decisions thermometer encoded**

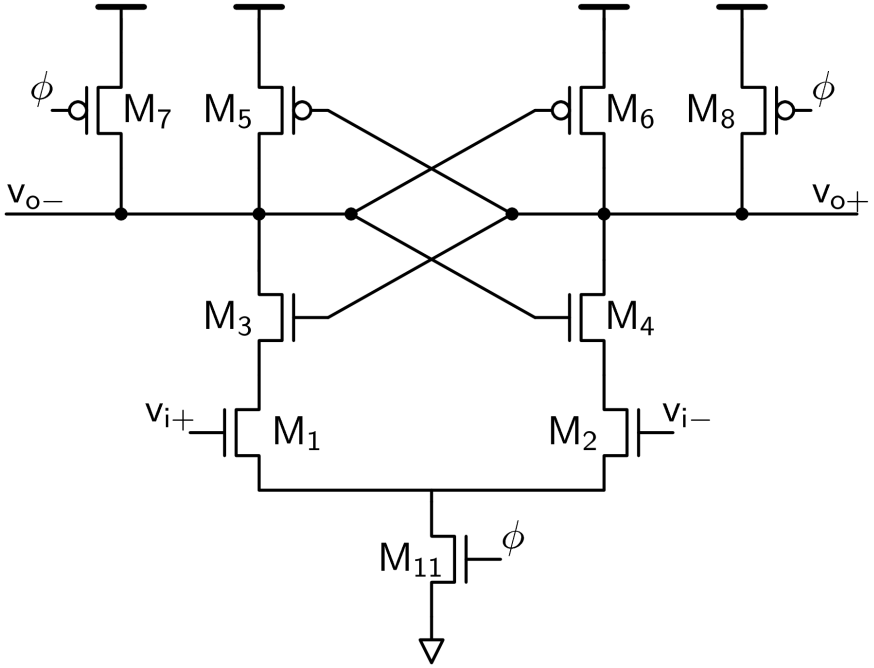
Output Range Enhancement

- 9 Bit Decision Comparators per stage (3.3 bits/stage)
- 4x gain per stage (1.3 bit redundancy)
- Reference voltages set to power supply levels
- Input range is 83% the reference range
- Output range is 33% the reference range



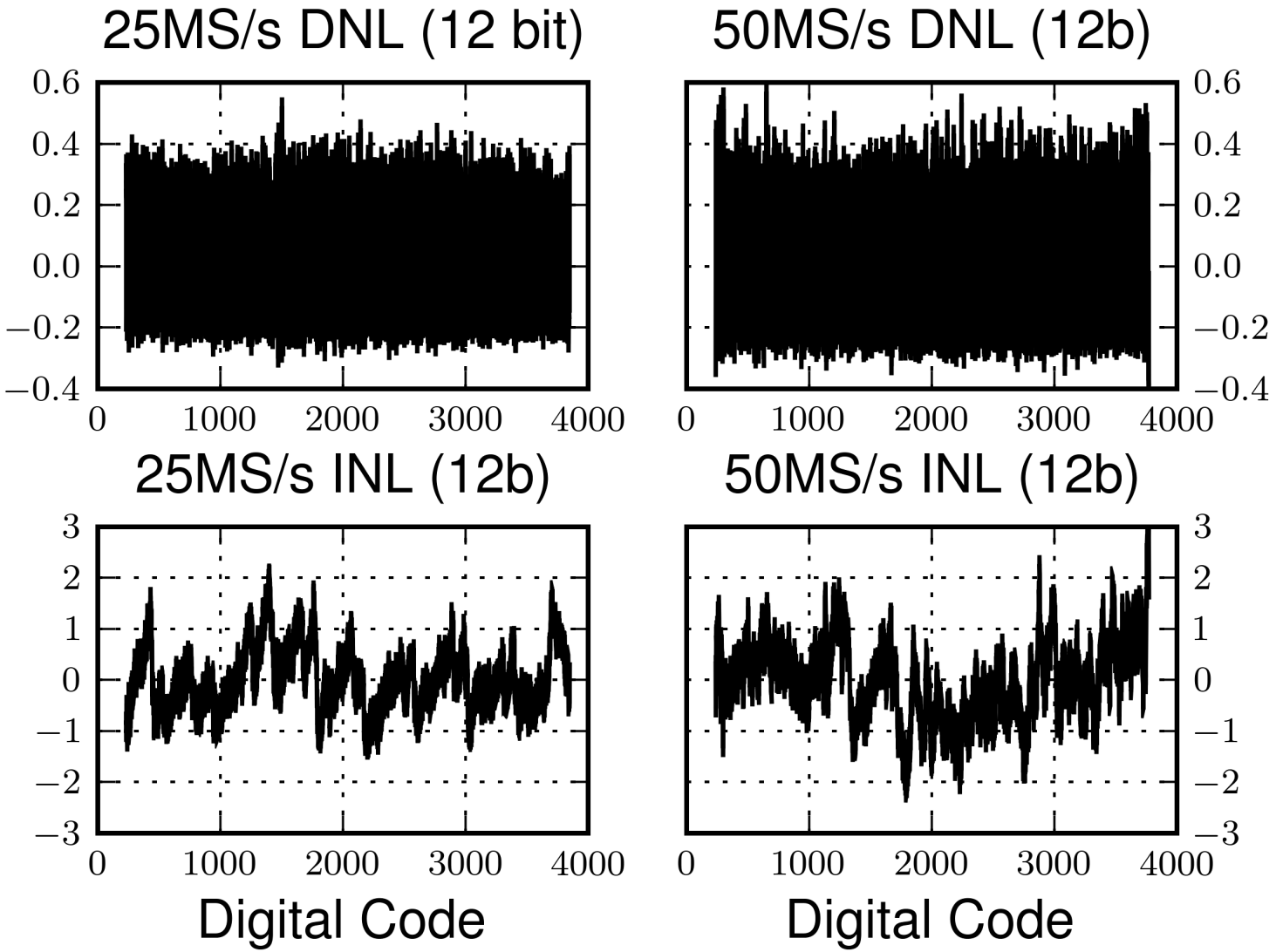
Bit Decision Comparator (BDC)



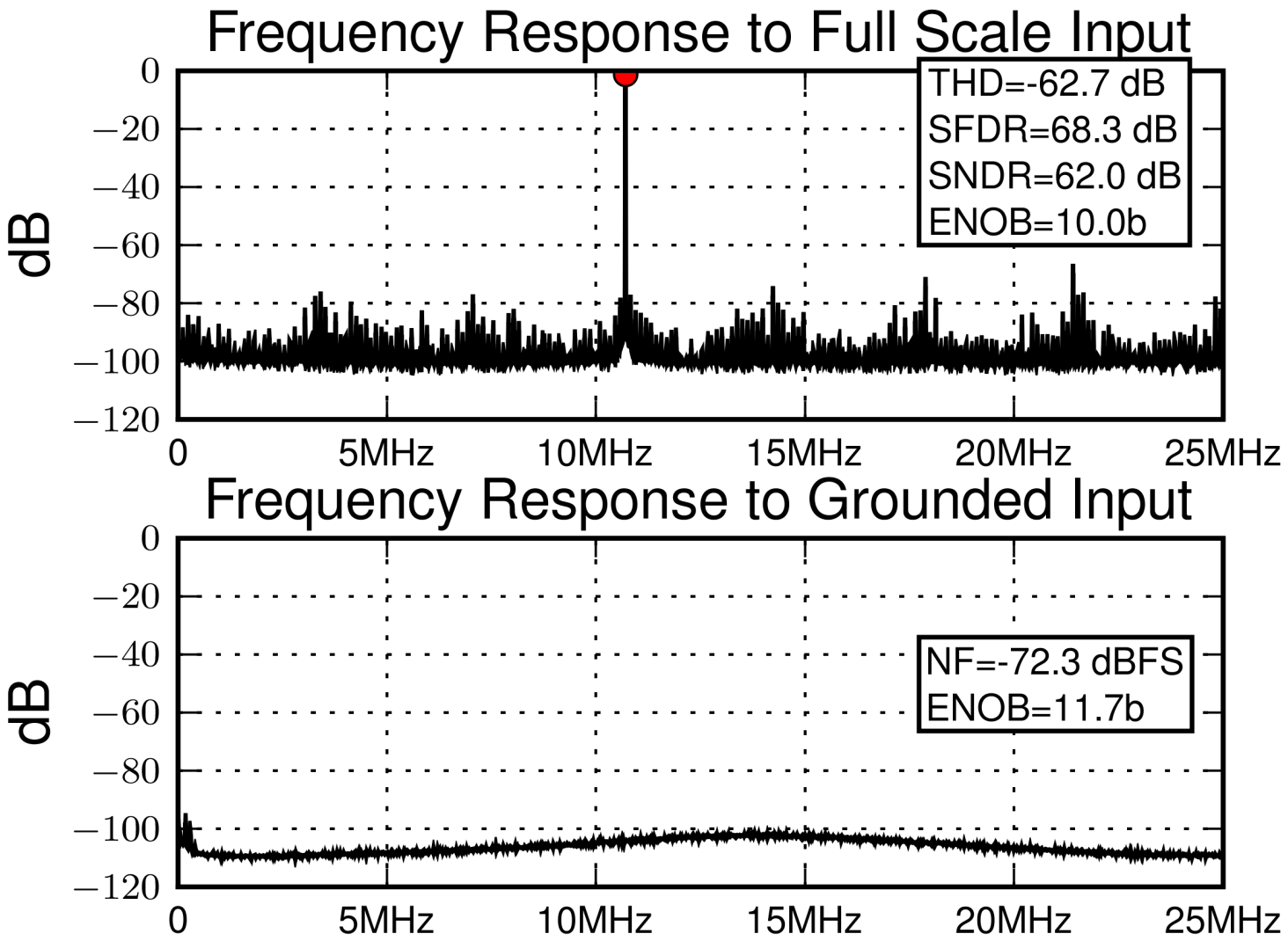


- **BDC offsets were larger than predicted**
- **BDC offset limits overall linearity**

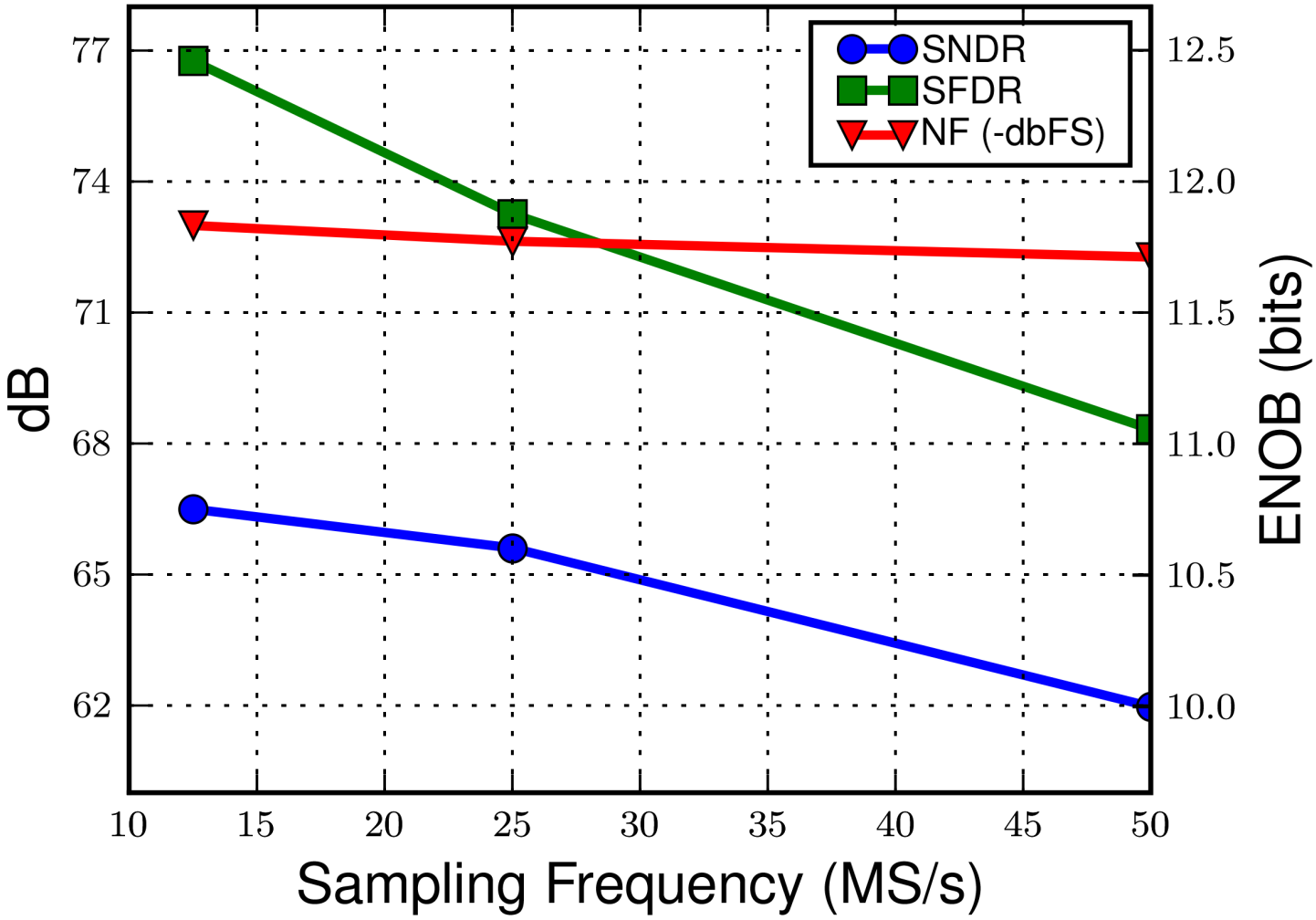
Linearity


25MS/s DNL (12 bit)
50MS/s DNL (12b)
0.6
0.4
0.2
0.0
−0.2
−0.4
0
1000
2000
3000
4000
25MS/s INL (12b)
50MS/s INL (12b)
3
2
1
0
−1
−2
−3
Digital Code
Digital Code

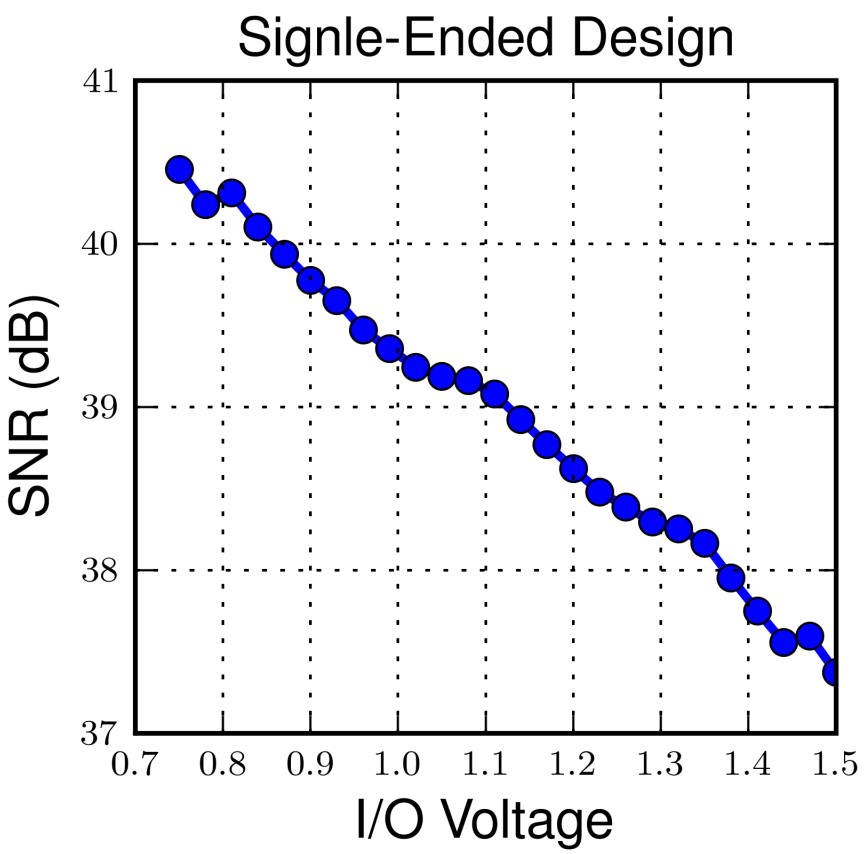
50MS/s Frequency Response

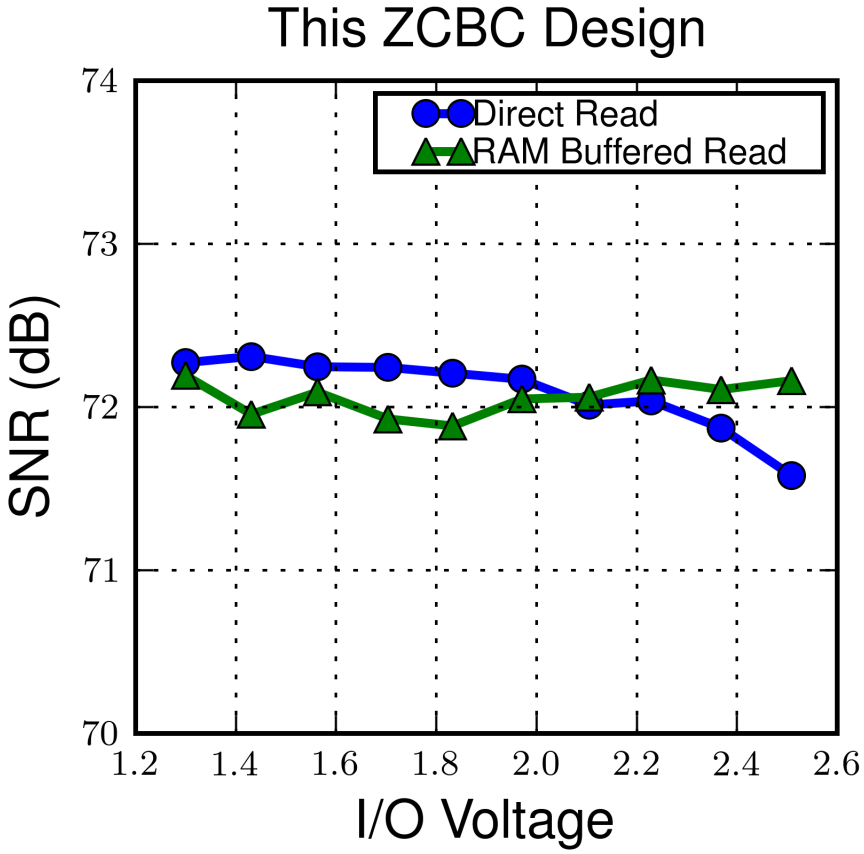


Performance vs Sampling Freq.



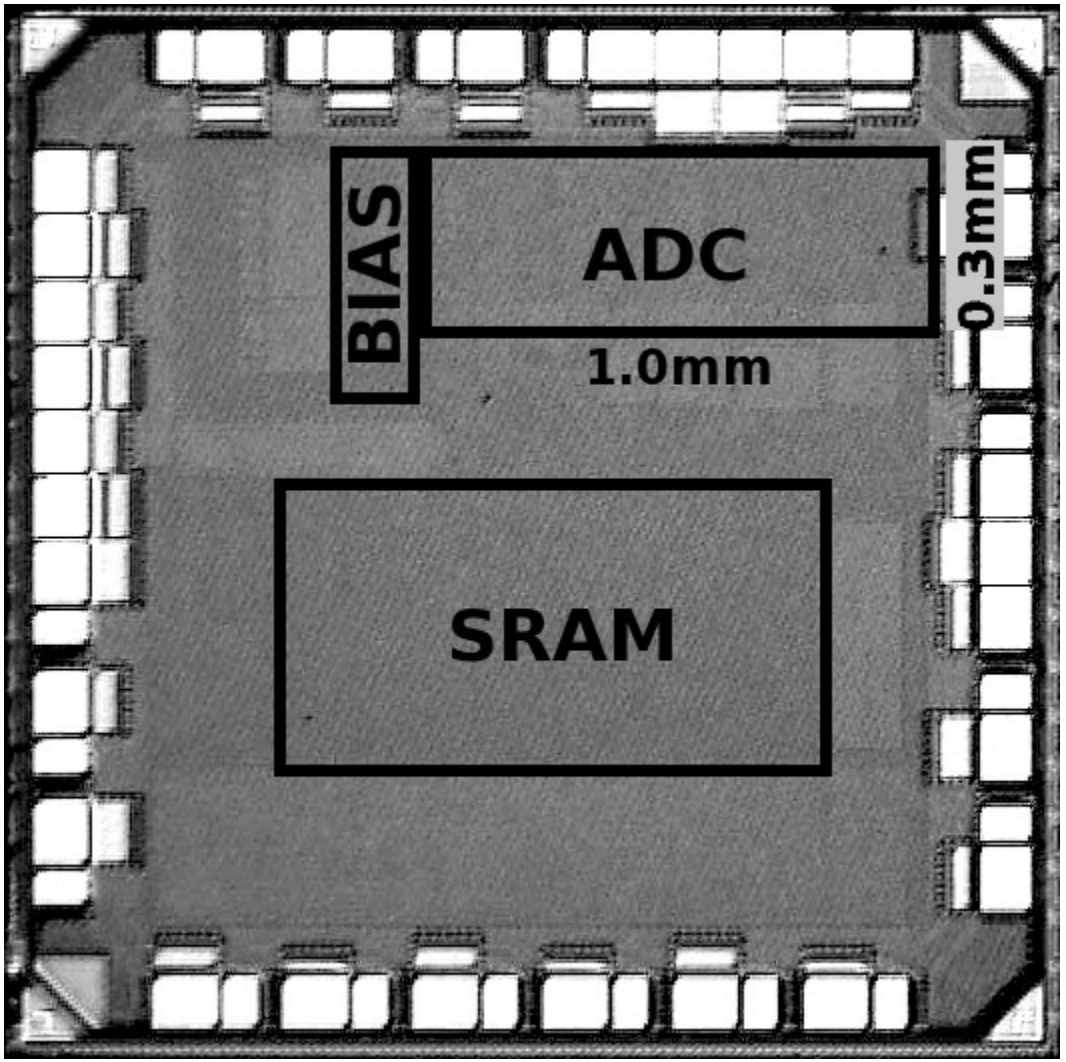
SNR Sensitivity To I/O Voltage





Chip Micrograph

- 90nm CMOS
- 0.3mm^2



Performance Summary

Technology	90nm CMOS	
Area	0.3 mm^2	
Input Voltage Range	2V (differential)	
Power Supply	1.2V	
Sampling Frequency	25MS/s	50MS/s
Differential Non-linearity	±0.5 LSB_{12}	+0.68/-0.4
DNL/INL	±2.0 LSB_{12}	+3.0/-2.7
Power Consumption	3.8mW	4.5mW
Dynamic Range	72dB	72dB
SFDR	73dB	68dB
SNDR	66dB	62dB
ENOB	10.6b	10.0b
Figure of Merit	98 fJ/step	88 fJ/step

FOM Comparison

Resolution (Bits)	ENOB (Bits)	Sampling Rate(MS/s)	FOM (fJ/step)	Type	Year
13	10.5	250	280	Pipe	VLSI ‘08
12	10.5	20	310	Pipe	ISSCC ‘08
12	10.3	50	360	Pipe	VLSI ’08
12	10	40	389	Pipe	VLSI ‘07
12	10	50	88	Pipe	This work

- Complete list of published non-interleaved ADC’s with FOM < 500fJ/step and ENOB ≥ 10 Bits, through 2008

- Excludes delta-sigma converters and converters with sampling rates < 1MS/s

Conclusions

- **Demonstrated a 12b, 50MS/s Pipelined ADC:**
  - **Zero-crossing based circuit**
  - **Fully differential signal path**
  - **No CMFB required**
  - **Chopper offset compensation**
  - **Split reference voltage switching scheme**
  - **Output range enhancement**

Acknowledgements

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