A Zero-Crossing-Based 8-bit 200 MS/s Pipelined ADC

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***Abstract*—Zero-crossing-based circuits (ZCBC) are introduced as a generalization of comparator-based switched-capacitor circuits (CBSC). To demonstrate this concept, an 8-bit, 200 MS/s, pipelined ADC is implemented in a 0.18 μm CMOS technology. A dynamic zero-crossing detector and current source replace the functionality of an opamp to realize a precision charge transfer. Furthermore, current source splitting improves linearity at high speeds and bit decision flip-flops replace traditional bit decision comparators for increased speed. The complete ADC draws no static current and consumes 8.5 mW of power. The corresponding FOM is 0.38 pJ/step at 100 MS/s and 0.51 pJ/step at 200 MS/s.**

***Index Terms*—Analog-to-digital conversion (A/D), analog-to-digital converter (ADC), comparator-based switched-capacitor circuits (CBSC), scaled CMOS, zero-crossing-based circuits (ZCBC).**

I. Introduction

TECHNOLOGY scaling is raising many issues for analog circuit design. Device leakage, mismatch, and modeling complexity are increasing while intrinsic device gain and voltage supplies are decreasing [1], [2]. For switched-capacitor circuit design specifically, decreasing device gain and voltage supplies are increasing the difficulty of realizing a precision charge transfer in the traditional manner via a high-gain, high-speed operational amplifier (opamp) in feedback.

Designing an opamp to maintain the necessary gain and bandwidth as device gain decreases can be done by cascading and/or cascoding gain stages. Cascading gain stages introduces complexity and issues of stability versus bandwidth/power consumption [3]. Cascoding, on the other hand, exacerbates the issues of voltage supply scaling as it reduces available signal swing. Such reductions in signal swing require a squared increase in capacitance and thus power consumption to maintain the same SNR.

It has been speculated that because of these issues it will be both economically and technically impossible to implement high resolution circuits such as data converters in low-voltage, deeply scaled technologies and that the optimality of "System on Chip" (SoC) integration may be ending in favor of "System in Package" (SiP) solutions, where functionality from different die are assembled in a single package [1]. The issues associated with taking signals "off-chip," however, greatly limit this approach, especially at higher speeds and resolutions.

Digital correction and calibration is area that is providing methods of dealing with the issues of technology scaling. The calibration ideas and methods demonstrated in [4], [5] have formed the basis for many techniques such as open-loop amplification [6], incomplete settling [7], and low-gain closed-loop amplification [8].

Another approach to dealing with device and voltage scaling is an alternative architecture called comparator-based switched-capacitor (CBSC) circuits that was introduced in [9]. This architecture replaces the function of the opamp with the combination of a comparator and current source to realize the same charge transfer as an opamp-based implementation. It completely eliminates opamps from the design and does not require stabilizing a high-gain, high-speed feedback loop. This not only reduces complexity but also eliminates the associated stability versus bandwidth/power tradeoff.

The work presented here builds on the concepts of CBSC by generalizing them to a architecture called zero-crossing-based circuits (ZCBC) [10]. This paper is organized as follows: Section II reviews opamp-based and CBSC architectures. Section III introduces the generalization to zero-crossing-based circuits. Section IV provides the implementation details of the ZCBC pipelined ADC. Section V details the experimental results, and Section VI discusses the power efficiency of this ZCBC implementation.

II. Background

A. Opamp-Based Switch Capacitor Circuits

A typical opamp-based switched-capacitor gain stage implementation is shown in Fig. 1. ϕ_1 and ϕ_2 are nonoverlapping clock phases. When ϕ_1 is high, the circuit is configured in the *sampling* phase and the input voltage v_I is sampled with respect to $\mathrm{V_{CM}}$ onto capacitors C_1 and C_2. When ϕ_1 falls and ϕ_2 rises, the circuit is configured in the *transfer* phase. The role of the opamp is to *force* the virtual ground condition by driving the output voltage v_O until the v_X node equals $\mathrm{V_{CM}}$. The accuracy of the transfer phase is determined by how well the virtual ground condition is realized. If the error in the virtual condition is not signal dependent, then an offset results that can be nulled with any number of auto-zeroing techniques [11]. When the error is signal dependent, gain errors and/or nonlinearities will result. In the case of an opamp-based implementation, finite open-loop opamp gain and insufficient settling are two effects which cause such signal dependent errors in the virtual ground condition.

In the case of finite opamp gain, the accuracy of the virtual ground condition is inversely proportional to the open-loop gain of the opamp. The gain, therefore, must be large enough to ensure the signal dependent error in the virtual ground condition is small enough for the specific application.

In the case of insufficient settling, the feedback loop must be given ample time to settle to avoid a signal dependent error in

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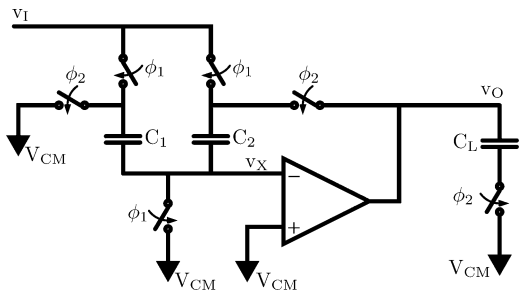

Fig. 1. Typical opamp-based switched-capacitor gain stage.

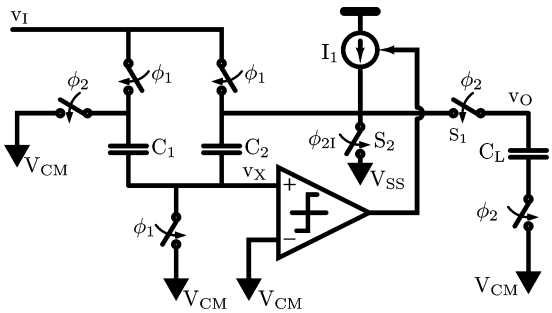

Fig. 2. Comparator-based switched-capacitor (CBSC) gain stage.

the virtual ground condition. The typical exponential settling of v_O and $v_{\rm X}$ in an opamp-based implementation is shown in the transient response of Fig. 3(a).

These issues create the stability versus bandwidth/power tradeoff for the opamp-based system because of the fundamental constraints associated with increasing gain and bandwidth simultaneously. Furthermore, the bandwidth requirements significantly decrease the power efficiency of an opamp-based system as the noise bandwidth of signal path is determined by the bandwidth of the feedback loop, which can be several times larger than the signal bandwidth to ensure sufficient settling time [7], [9].

B. Comparator-Based Switched-Capacitor Circuits

Comparator-based switched-capacitor (CBSC) circuits as shown in simplified schematic of Fig. 2 do not suffer from the above issues. Observe that the opamp is replaced with a comparator and current source. As with the opamp-based implementation, when ϕ_1 is high during the sampling phase, the input voltage v_I is sampled onto C_1 and C_2. When ϕ_2 goes high to enter the transfer phase, a short pulse ϕ_{2I} is used to initialize the charge transfer by closing switch $\rm S_2$ to pre-charge the output voltage v_O to ground. Following this pulse, $\rm S_2$ opens and the current source I_1 charges the capacitors to generate a constant voltage ramp on the output voltage v_O. This causes the virtual ground voltage $v_{\rm X}$ to ramp with it via the capacitor divider consisting of C_1 and C_2. As the voltage ramp proceeds, the comparator will *detect* when the virtual ground condition has been reached and then turn off the current source to realize the same charge transfer as the opamp-based implementation. The resulting transient response for voltages v_O and $v_{\rm X}$ is shown in Fig. 3(b).

It is important to realize that the shape of the transient response does not matter for switched-capacitor circuits. The

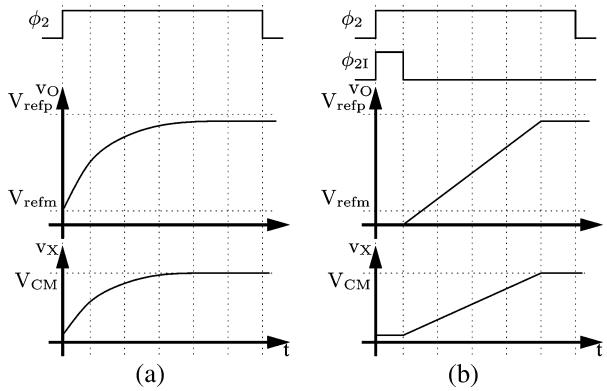

Fig. 3. Sample transient response of (a) an opamp-based and (b) a CBSC switched-capacitor gain stage.

critical time in the transfer phase is when the sampling switch opens to sample the output voltage v_O onto the load capacitor C_L. In fact, depending on the implementation of the opamp, two different opamp-based systems may have dramatically different transient responses depending on effects such as slewing and ringing. It is the accuracy of the virtual ground condition when the sampling switch opens that matters. Thus, whereas an opamp-based implementation forces the virtual ground condition, the CBSC implementation sweeps the output voltage and searches for the virtual ground condition. Both, however, realize the same charge transfer despite their dramatically different transient responses.

III. Zero-Crossing-Based Circuits

Just as the opamp in an opamp-based design, the comparator in a CBSC design contributes most significantly to the speed, power efficiency, and Figure of Merit (FOM) of the overall circuit. Generally, a comparator must resolve the difference between two arbitrary voltage waveforms. The input into the comparator of a CBSC circuit, however, is not arbitrary. As shown in the sample waveforms of Fig. 4, the input into the comparator of a CBSC circuit is a constant slope voltage ramp, so the comparator actually performs a uni-directional zero-crossing detection. Therefore, a general purpose comparator is not strictly necessary. This work generalizes CBSC circuits into zero-crossing-based circuits (ZCBC) by replacing the general purpose comparator with a zero-crossing detector. As discussed in Section VI, this generalization allows for implementations of zero-crossing detectors that are more power efficient than general purpose comparators.

Fig. 5 shows a simplified implementation of the zero-crossing-based circuit that is used in this work. The general purpose comparator of the CBSC implementation has been replaced with dynamic zero-crossing detector (DZCD) that consists of devices $\rm M_1$ and $\rm M_2$. The circuit functions similarly to the CBSC circuit shown in Fig. 2. During the sampling phase when ϕ_1 is high the input voltage is sampled onto C_1 and C_2. Then, as shown in the timing diagram of Fig. 6, ϕ_2 and ϕ_{2I} go high to start the transfer phase. ϕ_{2I} turns on $\rm M_4$ to pre-charge the output voltage v_O to ground. This pushes the virtual ground node voltage $v_{\rm X}$ down to turn off $\rm M_1$. Simultaneously, $\bar{\phi}_{2I}$ turns on $\rm M_2$ to pre-charge the voltage v_P high and turn on the

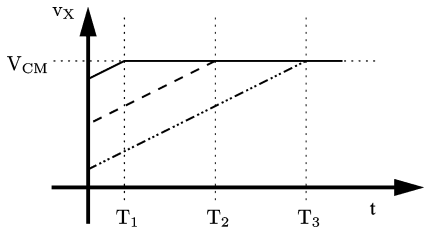

Fig. 4. Sample input waveforms into a CBSC comparator.

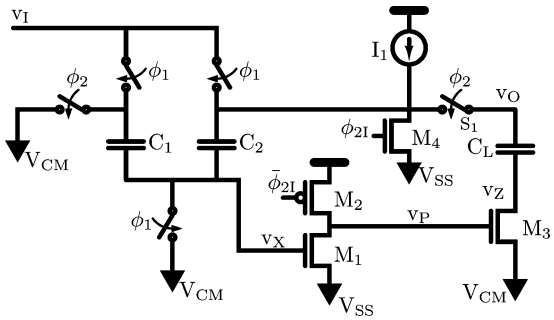

Fig. 5. Zero-crossing-based switched-capacitor gain stage.

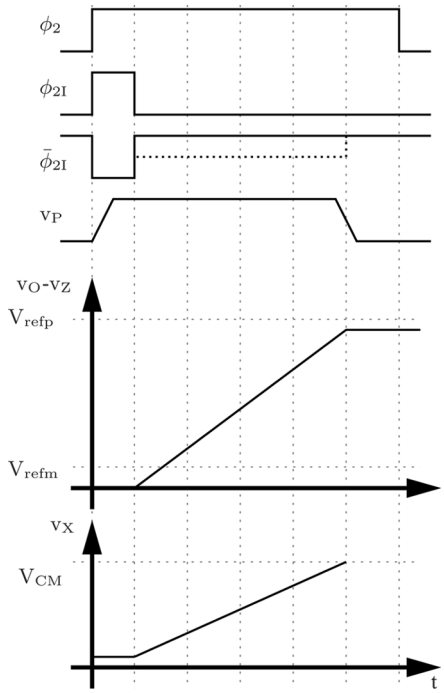

Fig. 6. Sample transient response of a ZCBC switched-capacitor gain stage.

sampling switch $\mathrm{M_3}$. This initializes the load capacitor C_L below the full scale output range.

When ϕ_{2I} drops, node v_P is left floating high to keep the sampling switch on, and the output voltage v_O begins to ramp from the current source pulling it up. v_X ramps with it according the capacitor divider established by C_1 and C_2. As v_X ramps up it will at some point give $\mathrm{M_1}$ sufficient gate drive to start pulling down the floating v_P node. When v_P is pulled down sufficiently to turn off the sampling switch $\mathrm{M_3}$, the voltage on the load capacitor C_L is sampled and the charge transfer is complete. Opening $\mathrm{M_3}$ to define the sampling instant minimizes signal dependent charge injection by performing bottom plate sampling [12].

The dynamic zero-crossing detector consisting of $\mathrm{M_1}$ and $\mathrm{M_2}$ is not suitable as a general purpose comparator. It can not detect differences in two arbitrary voltages. It is, however, suitable as a zero-crossing detector in this architecture because the constant slope voltage ramp created by the current source I_1 ensures that $\mathrm{M_1}$ switches consistently at the same voltage. The switching threshold of $\mathrm{M_1}$ is temperature, process, and ramp-rate dependent, but since the switching threshold is not signal dependent, it creates a constant offset that can be nulled with any number of traditional auto-zeroing circuits [11]. This initial implementation did not employ an auto-zeroing technique but rather globally adjusted the $\mathrm{V_{CM}}$ voltage externally to null the cumulative offset of the complete ADC. It must be noted, however, that power efficient auto-zeroing techniques need to be developed for this architecture to take the full advantage of the power efficiency of the DZCD.

One significant limitation to this DZCD is that it is inherently single-ended and does not have a natural differential extension. Thus, depending on the amount of power supply and substrate noise present in a particular system, this architecture may be not be suitable for high resolution applications.

Despite these limitations, this DZCD has several compelling advantages. It is fast, simple, and amenable to scaling. It produces a rail-to-rail digital logic level in a single stage while drawing no static current. It consumes only the power necessary to switch the capacitance on node v_P, which will be shown in Section VI to offer an improvement in power efficiency.

IV. ZCBC Pipelined ADC Implementation

A 1.5 bit/stage pipelined ADC was implemented to demonstrate this ZCBC architecture. The schematic of two adjacent stages (stages k and $\mathrm{k}+1$) is shown in Fig. 7 where the simplified gain stage shown in Fig. 5 has been split to form two pipeline stages. The sampling capacitors C_3 and C_4 in stage $\mathrm{k}+1$ become the load capacitor of stage k. The implementation details that follow apply to the general case when stage k is not the first stage. The subtle differences imposed on the first stage are discussed in Section IV-G.

A. DZCD Design

One significant issue that arises when v_P is left to float while the v_X voltage ramps is that feed-through from the C_gd of $\mathrm{M_1}$ pushes a signal dependent amount of charge onto the v_P node. This charge has to be removed by $\mathrm{M_1}$ when it switches and creates a signal dependent delay. Such a signal dependent delay produces a gain error similar to capacitor mismatch at the output. To eliminate this issue, rather than turning $\mathrm{M_2}$ off completely while the voltage ramps, the gate of $\mathrm{M_2}$ is biased so that $\mathrm{M_2}$ can sink the feed-through current and prevent v_P from accumulating a signal dependent amount of charge. The dashed line for $\bar{\phi}_{2I}$ in the timing diagram of Fig. 6 shows this scenario. After v_P switches, however, $\mathrm{M_2}$ is shut off to ensure no static current is drawn.

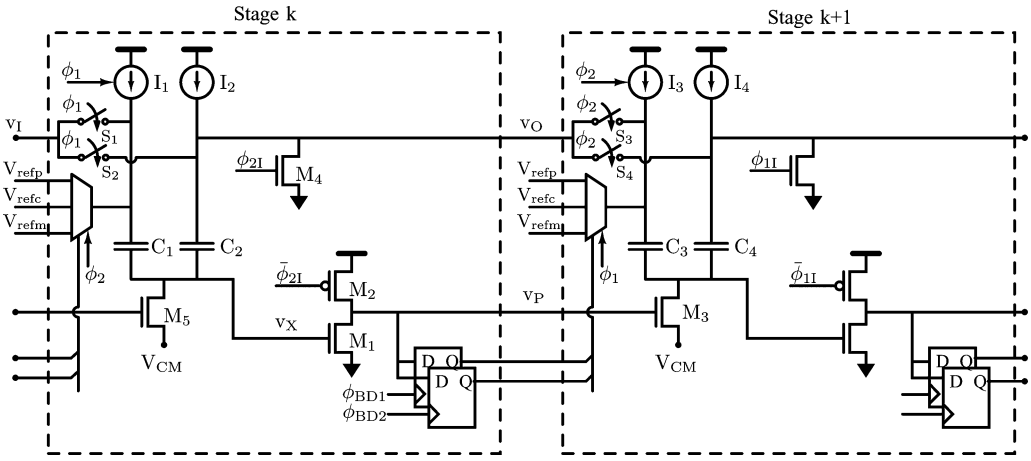

Fig. 7. Two stages of the 1.5 bit/stage zero-crossing-based pipelined ADC.

B. Current Source Splitting

The single current source I_1 shown in Figs. 2 and 5 has been divided in this implementation into I_2, I_3, and I_4 to charge each capacitor separately. This removes the series switch S_1 in Figs. 2 and 5 and improves the linearity and output swing. When implemented as a single current source, the charging current must pass through the series switch, which creates a voltage drop due to the finite on-resistance of the switch. This voltage drop reduces the output swing. More importantly, however, since the on-resistance of a typical CMOS switch is not constant, the voltage drop is also not constant and creates a signal dependent nonlinearity at the output. Since the ramp rate must be increased as the speed of the ADC increases, this problem gets worse as the ADC runs faster. Rather than sizing the switches up to reduce the on-resistance to acceptable levels, one can divide the current sources up as shown in Fig. 7 and remove the series switches to eliminate this issue. Since all other switches are connected to DC voltages, they do not produce signal dependent voltage drops and do not contribute nonlinearities to the output.

C. Shorting Switches

When dividing the current source, current mismatch and capacitive load differences will create different voltage ramp rates on each capacitor. Shorting switches S_1, S_2, S_3, and S_4 of Fig. 7 have been added to carry any mismatch current to ensure that each capacitor charges at the same rate. When ϕ_1 is high, stage k is in the sampling phase and I_2 charges C_2 directly. When ϕ_2 is high, stage k is in the transfer phase and I_2 charges half the capacitive load because C_1 and C_2 are configured in series.[1] To maintain the same voltage ramp rate, the charging current provided by I_2 should be reduced by two during the transfer phase. For this implementation the charging current of I_2 was not changed between the sampling and transfer phases for simplicity. This means that the 1/5 the current supplied by I_2 during the transfer phase actually goes through each of the shorting switches S_3 and S_4 to keep the voltage ramp rate constant. Thus, in this implementation, the sizing requirement of the switches was reduced by a factor of 5 over using a single current source and a single series switch.

To further reduce the sizing of the shorting switches, these switches were implemented as nMOS only switches with a gate boosting circuit shown in Fig. 8. The corresponding timing diagram is shown in Fig. 9. In the schematic, M_1 is the actual shorting switch, and the remaining circuitry is the driver. During the pre-charge phase when ϕ_{2I} is high, the source and drain of M_1 is reset to ground. Simultaneously the gate is charged to V_{DD} via M_2. Since M_2 is an nMOS, its gate voltage must be boosted to give it sufficient gate drive to switch it to V_{DD}. This boosted gate drive is generated via the global switch driver circuit also shown in Fig. 8. This circuit is based on the circuits found in [13], [14], and it ensures no device is stressed above the supply voltage. So during the pre-charge phase, C_1 is charged to V_{DD}. When ϕ_{2I} drops to end the pre-charge phase, the gate of M_1 is left floating. Since the source and drain of M_1 are connected to the output voltage of the ZCBC stage, they will then begin to ramp due to the current sources charging the sampling capacitors. The feed-through from C_1 will pull the floating gate with them as they ramp and provide a constant V_{GS} of V_{DD} on M_1. A constant V_{GS} provides a much more constant resistance than a complementary switch and thus further reduces the sizing requirements of the shorting switch. At the end of the transfer phase when ϕ_1 rises, M_4 discharges the floating gate and turns off the shorting switch. M_3 ensures that the source-drain voltage of M_4 never exceeds V_{DD} and no devices are stressed above their voltage rating.

Two global switch drivers as shown in Fig. 8 are implemented on chip and shared between all the shorting switches of all the stages of the same phase. Current source splitting and switch gate boosting allow for minimum sized nMOS shorting switches.

D. Reference Voltage Switches

The reference voltage multiplex switches ($\mathrm{V}_{\mathrm{refx}}$ switches in Fig. 7) subtract the quantized voltage from the input to produce the residue. In the case of a 1.0 bit/stage implementation, they

[1]This discussion applies to the case of a uniformly scaled 1.5 bit/stage ADC where the sampling capacitors are equal and $C_1 = C_2 = C_3 = C_4$. The exact numbers change depending on stage scaling or resolution when the sampling capacitors are not equal, but the technique still applies.

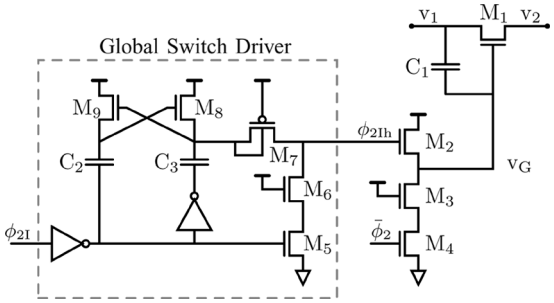

Fig. 8. Shorting switch implementation.

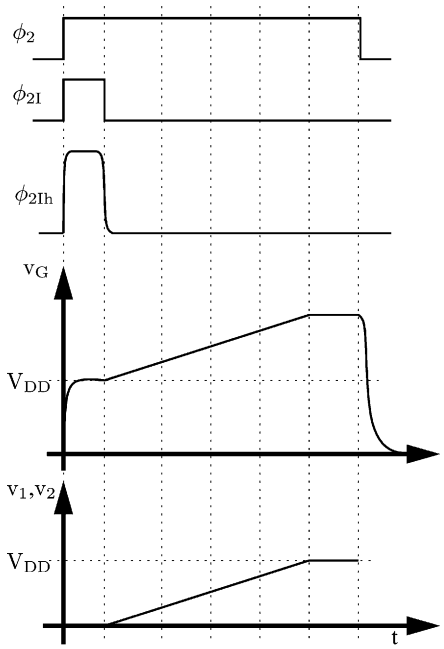

Fig. 9. Shorting switch timing diagram.

only switch between two voltage levels, and thus they are inherently linear. In the case of a 1.5 bit/stage implementation, however, they must switch between three different reference voltages, and a nonlinearity can result if the reference voltages themselves are nonlinear. In the case of an opamp-based implementation, the feedback loop must settle and thus the voltage drop across the reference switches is not a significant issue. In this ZCBC implementation, however, there is a constant current through the $\mathrm{V_{refx}}$ switches that produces a voltage drop due to its finite resistance. If each switch has a different resistance, then each will have a different voltage drop and create a nonlinearity at the output. To ensure sufficiently matching switch resistance, the gate boosting circuit described in [14] is used to implement the $\mathrm{V_{refx}}$ switches. This circuit does not reduce reliability as it ensures that no device is stressed above the power supply and it boosts the gate to ensure each switch has the same $\mathrm{V_{GS}}$. This same circuit is also used for the input sampling switch.

E. Current Source Implementation

The current sources (I_1, I_2, I_3, and I_4 of Fig. 7) were implemented as pMOS cascoded current sources as shown in Fig. 10. The cascode device also doubles as the enable switch. Sufficient settling of the cascode voltage on the gate of $\mathrm{M_2}$ is not difficult

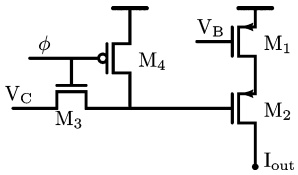

Fig. 10. Current source implementation.

to achieve when the enable is overlapped with the pre-charge phase. Not only does this give it extra time to settle but the pre-charging of v_O pulls the drain down and the feed-through from the C_{gd} of $\mathrm{M_2}$ helps its gate reach the cascode bias level faster.

In Appendix B the actual gain of the ZCBC amplification stage is calculated when including the effects of finite output impedance in the current sources and finite delay in the DZCD. The result when $C_1 = C_2$ is

$$v_O = \frac{2}{1 + \frac{\Delta_{vo}}{V_A}} v_I \tag{1}$$

where V_A is the effective Early voltage of the current source and Δ_{vo} is the residual overshoot of the output voltage due to the finite delay of the zero-crossing detector. The residual overshoot can be expressed mathematically as

$$\Delta_{vo} = a_0 t_d$$

where a_0 is the baseline output voltage ramp rate and t_d is the delay of the zero-crossing detector (see (14)). Because the DZCD has finite delay and because the finite output impedance of the current source causes the ramp rate to change, the amount of overshoot when the DZCD switches will be output voltage dependent. Equation (1) reveals that this overshoot lowers the gain of the ideal ZCBC gain stage in a manner similar to finite opamp gain in an opamp-based system. When used in a pipelined ADC, this produces static nonlinearities at the bit decision boundaries.

This error changes with the overall speed of the ADC. The ramp rate must be changed proportionally with ADC speed, and the delay of the zero-crossing detector used in this design decreases by the cube root of the square of the ramp rate (see (14)). The net effect is that the overshoot Δ_{vo} will change by the cube root of the ramp rate. So as one increases the speed of the ADC the overall linearity will get worse by a cube root factor.

The designer must ensure that the voltage ratio Δ_{vo}/V_A is sufficiently small to meet the desired ADC resolution. For example, in a 10 bit, 1 bit/stage pipeline ADC, with $\Delta_{vo} = 100\ \mathrm{mV}$, V_A must be 100 V for a 1/2 LSB DNL error. Alternatively, one can use any number of the digital calibration techniques for removing such static nonlinearities that result from this effect such as those used in [4], [5].

F. Bit Decision Flip-Flops

The bit decision comparators of the sub-ADC of a pipelined ADC provide a coarse quantization of the output voltage v_O and are traditionally implemented as clocked comparators. When the bit decision comparators are implemented in this manner in ZCBC architectures, they lie in the critical path because they

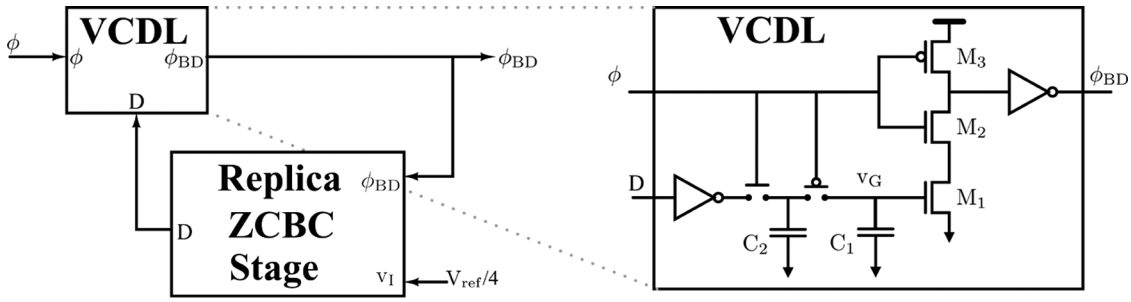

Fig. 11. The bit decision flip-flop phase generation circuit, including the voltage-control delay line implementation.

must make their decision after one stage completes its transfer and before the next stage can begin. Thus they can limit the overall speed of the ADC and create meta-stability issues when they are not given ample time to make their decision. To remove the bit decision logic from the critical path, this design does not use traditional bit decision comparators but rather uses bit decision flip-flops as shown in Fig. 7.

Since the output voltage v_O ramps up linearly until the DZCD switches, the time at which the DZCD switches is proportional to the output voltage. Therefore, in a manner analogous to a single slope ADC, sampling the DZCD output with flip-flops whose sampling clock is phase-aligned with the appropriate decision threshold yields an equivalent coarse quantization of the output voltage.

To generate the clock phase that corresponds to the desired $\pm V_{ref}/4$ bit decision levels necessary for a 1.5 bit/stage ADC, the feedback circuit of Fig. 11 is used. The clock ϕ goes through a voltage-controlled delay line (VCDL) to produce the reference clock phase ϕ_{BD}. ϕ_{BD} along with the bit decision voltage $V_{ref}/4$ goes into a replica pipeline stage, and the output bit of this replica stage is then fed back to the VCDL to adjust the phase of ϕ_{BD} for the next sample.

The actual circuit implementation of the VCDL is also shown in Fig. 11. The voltage v_G controls the delay of the current-starved inverter consisting of M_1, M_2, and M_3. Suppose v_G starts at V_{DD} such that C_1 is fully charged. This gives the VCDL minimal delay and causes the bit decision flip-flop in the replica stage to sample the DZCD output immediately to yield a high decision output D. This will cause the VCDL to discharge C_2 to ground. When ϕ falls, C_1 and C_2 get shorted together to decrement the voltage v_G on C_1 and increase the delay. On each clock cycle the delay will continue to increase until the phase of ϕ_{BD} passes the $V_{ref}/4$ threshold and causes the bit decision flip-flop in the replica stage to sample the low DZCD output. At that point C_2 will be charged to V_{DD} and when ϕ falls and C_2 and C_1 are shorted, v_G will increment to decrease the delay. In steady state the bit decision flip-flop of the replica stage will toggle high and low to keep ϕ_{BD} aligned to the falling edge of the DZCD in the replica stage. The small amount of jitter from such toggling is not an issue due to the over-range protection offered by a 1.5 bit/stage ADC. The over-range protection also eliminates any offset differences between the flip-flops of the replica stage and the actual pipeline stages from being problematic.

Using bit decision flip-flops removes the bit decision logic from the critical path because the bit decisions are made in parallel with the voltage ramp and are ready by the time the voltage ramp ends. This removes the meta-stability issues that can arise from using traditional clock comparators. Furthermore, the bit decision flip-flops do not have any unusual requirements and can be taken from a digital standard cell library.

G. First Stage Considerations

Since the first pipeline stage is not driven by a ZCBC stage, it requires several slight modifications to the schematic shown in Fig. 7. The input voltage v_I of the first stage is not a voltage ramp but the actual low-impedance ADC input. This means that current sources I_1 and I_2, which generate the voltage ramp during the sampling phase, are not needed. I_1 can be removed completely. I_2 is still needed during the transfer phase when ϕ_2 goes high, so it is implemented as an enabled current source for the first stage. Furthermore, the first stage does not have a previous stage to control the sampling switch (M_5 of Fig. 7) and the V_{refx} switches. Since the sampling capacitors are driven with a low-impedance source, the gate of the sampling switch of the first stage is tied to ϕ_1 to give maximum settling time and to perform bottom-plate sampling. Lastly, without a voltage ramp input and a zero-crossing detector, bit decision flip-flops cannot be used to drive the analog multiplexer of the first stage. Therefore, traditional clocked comparators are used for the first stage and the input sampling period of the gate-boosted nMOS sampling switch is reduced to give them ample time to make their decision. Since the input switch does RC sampling, this reduction in time is not an issue.

V. Experimental Results

This design was implemented as ten equally sized pipeline stages in a 0.18 μm CMOS technology in an active die area of 0.05 mm^2. The die photo is shown in Fig. 12. Fig. 13 shows the DNL and INL is $\pm$0.5 LSB and $\pm$0.75 LSB at 100 MS/s and $\pm$0.75 LSB and $\pm$1.0 LSB at 200 MS/s. Fig. 14 shows the frequency response to a near Nyquist rate input tone for 100 MS/s and 200 MS/s. From the frequency response the ENOB is measured at 6.9 bits and 6.4 bits for 100 MS/s and 200 MS/s respectively. The spectral response carries many aliased harmonics due to static nonlinearities that cause distortion, but these harmonics carry very little power. The SNDR is dominated by temporal circuit noise as is further discussed in Section VI-C.

The power consumption is plotted as a function of sampling frequency in Fig. 15. At 200 MS/s the ADC consumes 8.5 mW (2.9/5.6 mW analog/digital) from a 1.8 V power supply. Fig. 15

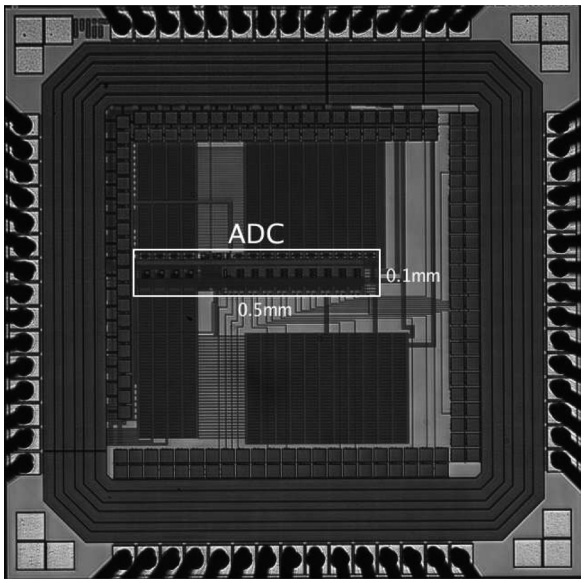

Fig. 12. Die photo of 0.05 mm^2 ADC in 0.18 μm CMOS.

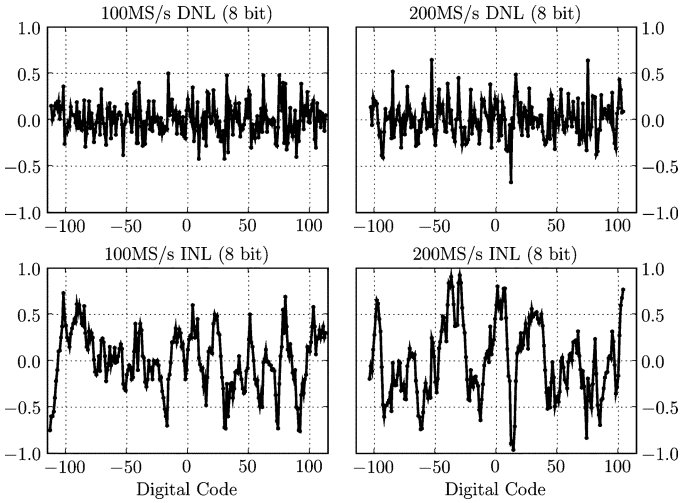

Fig. 13. DNL and INL plots for 100 MS/s and 200 MS/s operation.

shows that the complete ADC draws only dynamic power. The current sources do not draw static power because they provide only the charge necessary to realize the charge transfer and then turn off.

The corresponding Figure of Merit ($\mathrm{FOM} = P/2f_{\mathrm{in}}2^{\mathrm{ENOB}}$) is 380 fJ/step at 100 MS/s and 510 fJ/step at 200 MS/s. These results are summarized in Table I.

VI. Power Efficiency Analysis

A. DZCD Noise Analysis

A thorough analysis of the noise performance of CBSC circuits, including the contribution of the threshold detecting comparator, current sources, and sampling switches, has been presented in [9], [15]. Like CBSC circuits, the most significant source of noise for this circuit is the DZCD. Noise from the DZCD causes timing jitter on the falling edge of v_P, which creates uncertainty in when the sampling switch opens. Because the sampling switch opens at an uncertain time, an uncertain

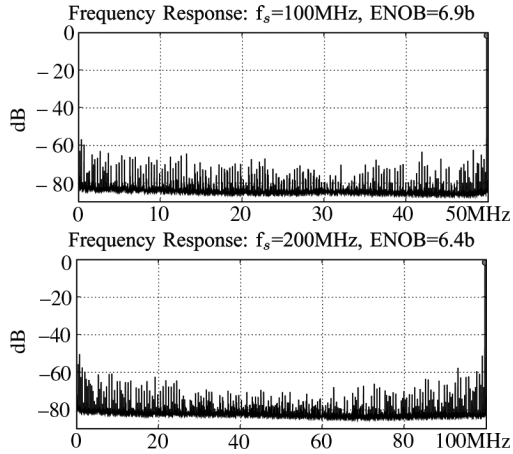

Fig. 14. Measure frequency response to near Nyquist rate input tone.

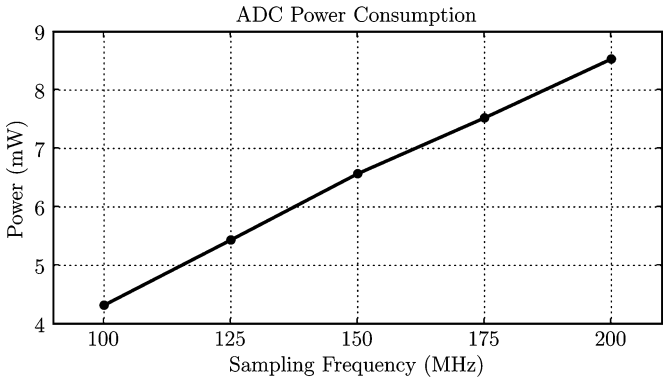

Fig. 15. Measured power consumption versus sampling frequency.

TABLE I
ADC Performance Summary

Technology	0.18μm CMOS	
Area	0.05 mm^2	
Input Voltage Range	1V (single ended)	
Power Supply: $\mathrm{V_{DD}}$	1.8V	
Sampling Frequency	100MS/s	200MS/s
DNL	$\pm$ 0.50 $\mathrm{LSB_8}$	$\pm$ 0.75 $\mathrm{LSB_8}$
INL	$\pm$ 0.75 $\mathrm{LSB_8}$	$\pm$ 1.00 $\mathrm{LSB_8}$
ENOB	6.9b	6.4b
Power Consumption	4.5mW	8.5mW
Figure of Merit: $\frac{P}{2f_{\mathrm{in}}2^{\mathrm{ENOB}}}$	0.38 pJ/step	0.51 pJ/step

voltage, or noise, will be sampled as the output voltage ramps. Device $\mathrm{M_1}$ of the DZCD in Fig. 7 contributes most significantly to this source of noise.

Fig. 16 shows the waveforms obtained from a transient simulation of a single pipeline stage. The waveform names correspond to voltages shown in the schematic of Fig. 7. The first waveform shows the transient response of ϕ_2 and ϕ_{2I}. The second plot shows the transient response of v_P, v_{X}, and v_O. The third plot shows I_{D}, the transient current drawn by $\mathrm{M_1}$. This current draw is insignificant while the voltage ramp proceeds until v_{X} gets high enough to start turning on $\mathrm{M_1}$. At

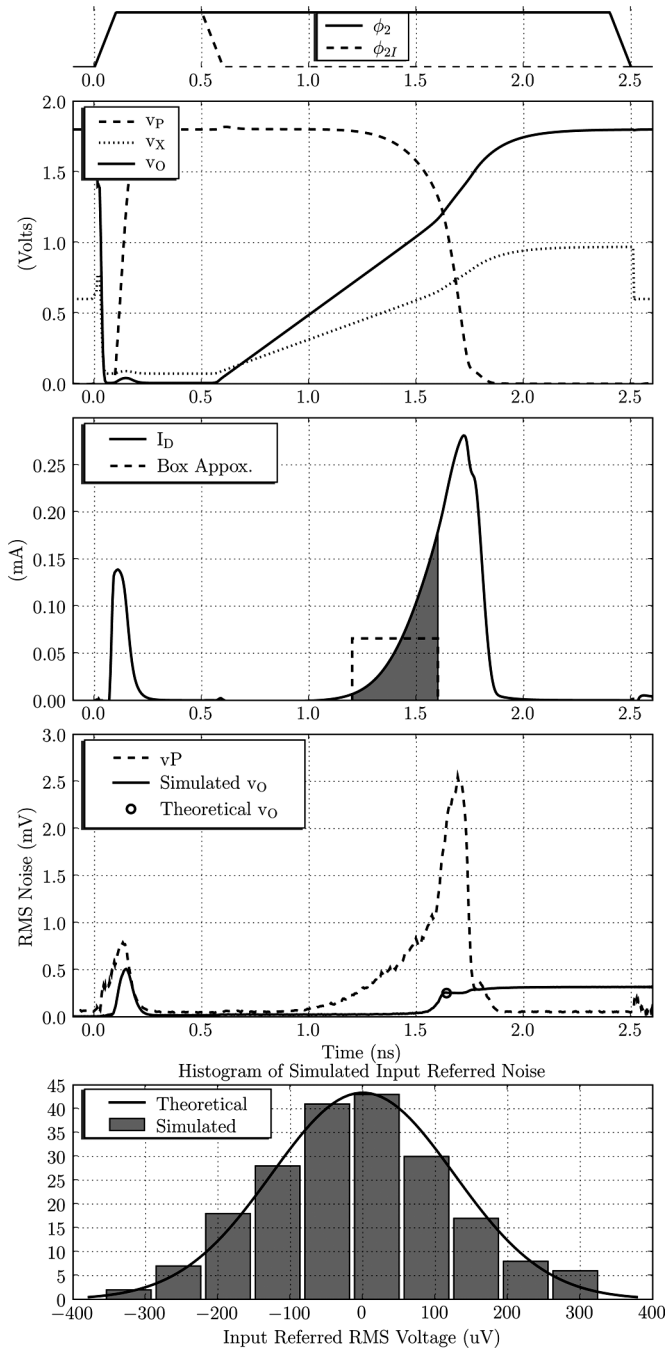

Fig. 16. Simulated transient response used for noise analysis verification.

that point the current level rises rapidly until v_P is completely discharged at which point the current draw returns to zero. The shaded area under the $I_{\rm D}$ waveform represents the total charge consumed while the sampling switch is closed (i.e. v_P is high enough to provide $\rm M_3$ sufficient gate drive to be on). It is during this period that the noise generated by $\rm M_1$ integrates onto the capacitance on node v_P and causes timing jitter on the falling edge of v_P.

Approximating the shaded area of the current spike as a box of equal area simplifies the noise calculation. If the height of this box is $\bar{I}_{\rm D}$ and the width is t_d, then the effective noise bandwidth is $1/2t_d$ and the input referred noise spectral density is $8kT/3\bar{g}_m$, where $\bar{g}_m$ is the transconductance resulting from a bias current of $\bar{I}_{\rm D}$ in device $\rm M_1$. The total input referred noise is the product of the bandwidth and the spectral density and equals

$$\bar{v}^2_{O,\rm ZCBC} = \frac{4kT}{3\bar{g}_m t_d}. \tag{2}$$

For this design with a ramp rate for 200 MS/s operation, simulation shows $t_d = 400$ ps and $\bar{g}_m = 870\ \mu$S. This gives 250 μV of RMS noise on the output.[2] To verify this result, a transient noise simulation was run with 200 parallel transient responses to yield the fourth plot of Fig. 16. The dashed line shows the RMS noise on v_P and the solid line shows the RMS noise on v_O as a function of time. The noise on v_O is insignificant until v_P switches to open the sampling switch. After the switch opens the output referred noise rises to 250 μV, which matches the theoretical calculation. In this simulation noise generation is enabled in all devices including the current sources and switches, and this verifies that the DZCD noise is the dominant source of noise.

The final plot of Fig. 16 shows the histogram of the input referred output voltage for the 200 parallel noise simulations. The theoretical Gaussian distribution is overlaid to show that the response is indeed approximated well by a Gaussian distribution. As shown in Appendix A, the box approximation for the $I_{\rm D}$ current pulse used in this analysis yields that same result as a more rigorous derivation using square-law device equations.

One additional source of noise that is investigated in [16] is the positive feedback loop that exists during the transient response from $\rm M_1$ through $\rm M_3$ and back through capacitors $C_{3,4}$ and C_2. The transient noise simulation for this implementation did not show this feedback loop contributed any significant increase in noise.

B. Comparison to Original CBSC Implementation

In the original CBSC implementation described in [9] a general purpose comparator was used for the zero-crossing detection. The first stage of this comparator was a differential pair with a constant bias current. It was shown in [9], [15] that for this setup the noise bandwidth is $1/2t_i$ where t_i is the delay of the first stage of the comparator and can be expressed as $t_i = \alpha(T_{CLK}/2)$. Both devices of the input pair contribute noise and thus the input referred noise spectral density is $16kT/3g_m$, where g_m is the transconductance of the input devices biased at $I_{\rm D}$. Thus the total noise for the original CBSC implementation is

$$\bar{v}^2_{O,\rm CBSC} = \frac{8kT}{3g_m t_i} \tag{3}$$

Since the static bias current drawn by the differential pair is $2I_{\rm D}$ for the entire half clock period $T_{CLK}/2$, the energy consumed by the input pair is

$$E_{\rm CBSC} = \rm V_{DD} I_D T_{CLK}. \tag{4}$$

[2]The RMS voltage is obtained by taking the square root of (2). To refer it to output requires multiplying the RMS noise by 2, which is the gain of the pipeline stage.

The energy consumed for this ZCBC implementation is

$$E_{\mathrm{ZCBC}} = \mathrm{V_{DD}}\bar{I}_{\mathrm{D}}t_d. \tag{5}$$

Multiplying the input referred noise together with the energy consumption gives a noise–energy product that tells how energy efficient each architecture is for a given noise. Assuming square-law device characteristics where $g_m = 2I_{\mathrm{D}}/(\mathrm{V_{GS}} - \mathrm{V_T})$, the noise–energy product (NEP) of the CBSC implementation can be calculated by multiplying (3) and (4) to give

$$\mathrm{NEP_{CBSC}} = \frac{8kT}{3\alpha}\mathrm{V_{DD}}(\mathrm{V_{GS}} - \mathrm{V_T}) \tag{6}$$

Likewise the NEP for this ZCBC implementation comes from multiplying (2) and (5) to give

$$\mathrm{NEP_{ZCBC}} = \frac{2kT}{3}\mathrm{V_{DD}}(\mathrm{V_{GS}} - \mathrm{V_T}) \tag{7}$$

When $\alpha = 1/2$, this ZCBC implementation operates $8\times$ more power efficiently than the original CBSC implementation for the same noise level. The original CBSC implementation, however, does have the capabilities to be made fully differential, which would improve a Noise-Energy product normalized to the signal energy by a factor of 4. However, this derivation does not include the power that the additional gain stages in the original CBSC implementation would consume.

The original CBSC used a two phase ramping scheme where first a fast ramp provided a coarse charge transfer and then a slower ramp followed to provide a fine adjustment. The two phase approach improved the power efficiency of the differential pair input stage. The DZCD used in this implementation, however, does not consume static power, and so the dual ramp scheme does not offer the same benefit. Furthermore, a single ramp scheme simplifies the design and enables higher speeds. The tradeoff for using a single ramp scheme is that the current levels are higher at the sampling instant. Higher currents can reduce linearity and output swing. Since neither linearity nor output swing were limiting issues in this implementation due to the circuit techniques described in Section IV, a single ramp scheme was used to take advantage of the complexity reduction and speed improvements.

C. FOM Discussion

Input referring the 250 μV of DZCD noise calculated in Section VI-A yields 125 μV, which for a 1 V full scale input corresponds to 69 dB of SNR (11 bit). The total input stage sampling capacitance is 50 fF, which corresponds to 287 μV of kT/C noise or 62 dB of SNR (10 bit). The total input referred noise is from both of these contributions would be 313 μV or 61 dB of SNR (9.8 bits). The measured SNR, on the other hand, is 40 dB (6.4 bit), which is more than a factor of 8 lower than the theoretical and simulated SNR, and this extra noise raises the FOM by the same factor. This extra noise is not likely fundamental but appears to be coming from power supply or substrate noise. As stated in Section III, the DZCD is inherently single-ended, giving it limited rejection from these sources. A strong correlation is found between the I/O output driver voltage level and the noise floor. This indicates that noise induced from the output drivers is at least one source of this extra noise. Improved I/O driver design, less inductive packaging, and deep N-well implants for better substrate isolation are options that could reduce the impact of this noise and yield a higher SNR and improved FOM.

Given the correlation between the I/O voltage level and the noise floor, one other potential noise source would be code dependent noise on the power supply, ground, substrate, reference voltages, or/and bias voltages due to the asynchronous switching of each ZCBC stage. For example, if the DZCD of one stage switches just before another, ground bounce from switching one stage may corrupt the other.

The power consumption for the reference and bias voltages of this implementation is ignored in the previous discussions because it is negligible as they are by-passed externally with large capacitors. In some applications, however, large external capacitors may not be practical and may require increased power consumption to generate the necessary reference and bias voltages.

The power consumption of the DZCD is simulated to be about 15% of the system power consumption. The digital power makes up approximately 66% of the total power consumption in this design. The Figure of Merit, therefore, for this implementation will improve in further scaled technologies as digital parasitic switching power consumption reduces. The rest of the power is consumed to switch various capacitors in the circuit including the sampling capacitors C_1, C_2.

VII. Conclusion

Zero-crossing-based circuits were introduced as a generalization of comparator-based switched-capacitor circuits. Zero-crossing-based circuits offer advantages over traditional opamp-based designs both from a theoretical power efficiency and from an amenability to scaling perspective. The implementation of an 8-bit, 200 MS/s pipelined ADC was presented that demonstrates this generalization. It includes a dynamic zero-crossing detector that is fast, simple, and power efficient. Furthermore, current source splitting was introduced as means of removing series switches to improve linearity and output swing. Bit decision flip-flops were also used in place of traditional clocked comparators to improve speed and eliminate meta-stability issues.

Appendix A
DZCD Noise Calculation

A more rigorous calculation of the noise due to the DZCD as expressed in (2) is presented here. This requires a transient noise analysis of device $\mathrm{M_1}$ of Fig. 5.

Suppose the input voltage v_{X} into the DZCD is a ramp with slope a. If $\mathrm{V_T}$ is the threshold voltage of $\mathrm{M_1}$, then the effective gate drive of $\mathrm{M_1}$ can be expressed as $v_e = v_{\mathrm{X}} - \mathrm{V_T}$. Assuming square-law device physics, the drain current of $\mathrm{M_1}$ can then be expressed as

$$I_D = \kappa v_e^2 \tag{8}$$

where $\kappa = \mu C_{ox}(W/2L)$.

By defining the time when $v_e = 0$ as $t = 0$, v_e can further be expressed as

$$v_e = at. \tag{9}$$

Substituting this into (8) gives

$$I_D = \kappa a^2 t^2 \tag{10}$$

and the transconductance of M_1 can be calculated from (8) and (9) as

$$g_m = 2\kappa a t. \tag{11}$$

Since the output voltage v_P is reset to $\mathrm{V_{DD}}$ during the initialization phase, v_P will be at $\mathrm{V_{DD}}$ at time $t = 0$. The drain current I_D will begin to discharge v_P at $t = 0$ according to the equation $v_P = \mathrm{V_{DD}} - (1/C_p)\int_0^t I_D dt$, where C_p is the parasitic capacitance on the v_P node. Defining $v_y = \mathrm{V_{DD}} - v_P$ yields the transfer function from the drain current I_D to the effective DZCD output voltage v_y as

$$v_y = \frac{1}{C_p}\int_0^t I_D dt. \tag{12}$$

Evaluating this integral with the results of (10) yields

$$v_y = \frac{\kappa a^2 t^3}{3C_p} \tag{13}$$

So the linear input voltage ramp ((9)) creates a squared current response ((10)) and a cubic voltage response ((13)) on the output.

Suppose the sampling switch M_3 of Fig. 5 has a switching threshold of $\mathrm{V_{DD}} - V_{tp}$. Then the time t_d at which the DZCD detector switches is the time when $v_y = V_{tp}$ and can be found by evaluating (13) at $t = t_d$ when $v_y = V_{tp}$ and solving for t_d. This gives

$$t_d = \sqrt[3]{\frac{3C_p V_{tp}}{\kappa a^2}}. \tag{14}$$

t_d is the time it takes M_1 to switch v_P from $\mathrm{V_{DD}}$ and turn off the sampling switch and is thus the delay of the DZCD.

It is the noise on the output voltage v_y at the sampling instant, which is time t_d, that matters in ZCBC circuits. This noise, however, is not stationary because the circuit is not in steady state. Since the channel current noise generated by M_1 is integrated to produce the output voltage, the noise will grow as a function of time as a random walk. Specifically, suppose the that noise spectral density of the channel current I_D is $N = (8/3)kTg_m$, then using the current to voltage transfer function of (12), the output noise at time t_d will be

$$\begin{aligned}\bar{v}_y^2 &= \frac{1}{C_p^2}\int_o^{t_d}\frac{N}{2}dt \\ &= \frac{8}{3}kT\frac{\kappa a t_d^2}{2C_p^2}\end{aligned} \tag{15}$$

From this result the input referred noise of the output voltage v_O can be calculated as

$$\bar{v}_{O,\mathrm{ZCBC}}^2 = \frac{\bar{v}_y^2}{A^2} \tag{16}$$

where A is the dynamic gain of the DZCD at time t_d. The dynamic gain is the ratio of the DZCD output voltage slope to the input voltage slope a evaluated at the switching time t_d. A can be expressed as

$$\begin{aligned}A &= \left.\frac{\partial v_y/\partial t}{\partial v_e/\partial t}\right|_{t=t_d} \\ &= \frac{\kappa a t_d^2}{C_p}.\end{aligned} \tag{17}$$

Furthermore, the mean transconductance from time 0 to t_d can be calculated from (11) as

$$\bar{g}_m = \kappa a t_d. \tag{18}$$

Combining (15) through (18) gives

$$\bar{v}_{O,\mathrm{ZCBC}}^2 = \frac{4kT}{3\bar{g}_m t_d} \tag{19}$$

which is the same result calculated using the approximations to yield (2). Following this same procedure under a velocity saturated region where $I_D \propto v_e$ also yields the same result.

Appendix B
ZCBC Gain Calculation

The current source used to generate the voltage ramp will have a finite output impedance, which means the ramp voltage a into the DZCD will not be constant. The current provided by I_1 in Fig. 5 can be approximated to first-order as

$$I(v_O) = I_0\left(1 - \frac{v_O}{V_A}\right) \tag{20}$$

where V_A is the effective Early voltage of I_1 and I_0 is the nominal current provided when v_O is at ground. This current is integrated onto the sampling capacitors during the transfer phase when ϕ_2 is high and results is an output voltage ramp rate of

$$\frac{\partial v_O}{\partial t} = \frac{I(v_O)}{C_T} \tag{21}$$

where $C_T = C_L + (C_2||C_1)$. The overshoot voltage v_{os} can be approximated as

$$v_{os} = t_d\frac{\partial v_o}{\partial t} \tag{22}$$

where t_d is the delay of the DZCD. Plugging the results of (20) and (21) into this result gives

$$v_{os} = \Delta_{vo}\left(1 - \frac{v_O}{V_A}\right) \tag{23}$$

where $\Delta_{vo} = I_0 t_d/C_T$ is baseline overshoot of the output voltage. The first term in this results produces a constant offset that is not output voltage dependent, so it can either be nulled with an auto-zeroing circuit or simply tolerated because it does not produce nonlinearities at the output. The residual overshoot, however, is the second term in this result and is $\Delta_{vo}(v_O/V_A)$.

This is output voltage dependent and cannot be nulled by auto-zeroing and will produce a nonlinearity at the output. Under ideal conditions and when $C_1 = C_2$, the gain of the ZCBC gain stage in Fig. 5 will be

$$v_O = 2v_I. \tag{24}$$

Subtracting the residual overshoot from the right hand side of the ideal result of (24) and solving for v_O gives

$$v_O = \frac{2}{1 + \frac{\Delta_{vo}}{V_A}} v_I. \tag{25}$$

This is the actual transfer function of the a ZCBC gain stage when one includes the effects caused by the finite delay of the zero-crossing detector and the finite output impedance of the current source. Note that the actual gain of the ZCBC gain stage is reduced from the ideal $2\times$ and that if the zero-crossing delay is 0 or if the output impedance of the current source is infinite there will be no error.

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