A 12b, 50 MS/s, Fully Differential Zero-Crossing Based Pipelined ADC

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Abstract—Zero-crossing based switch capacitor circuits have been introduced as alternatives to op-amp based circuits for eased design considerations and improved power efficiency. This work further improves the resolution, power efficiency, and robustness of previous zero-crossing based circuits (ZCBCs) and features a 90 nm CMOS, offset compensated, fully differential, zero-crossing based, 12b, 50 MS/s, pipelined ADC requiring no CMFB. The power consumption is 4.5 mW. The FOM is 88 fJ/step. Fully differential signaling is used to improve power supply rejection and power efficiency. A power efficient chopping offset compensation technique is presented. Reference voltage switching is improved to avoid gate boosted switches. Redundancy is used to reduce output range requirements for increased signal range. Two regenerative latch architectures used for bit decision comparison are analyzed and measured for offset, noise, and speed.

Index Terms—A/D, ADC, CBSC, chopper stabilization, chopping, CHS, comparator-based switched-capacitor circuits, offset compensation, scaled CMOS, ZCBC, zero-crossing based circuits.

I. INTRODUCTION

TECHNOLOGY scaling is raising many issues for analog circuit design. Device leakage, mismatch, and modeling complexity are increasing while intrinsic device gain and voltage supplies are decreasing [1], [2]. For switched-capacitor circuit design specifically, decreasing device gain and voltage supplies are increasing the difficulty of realizing a precision charge transfer via a high-gain, high-speed operational amplifier (op-amp) in feedback.

The two most important properties required from op-amps are high open-loop gain and stability under negative feedback. These requirements often conflict with each other and pose difficult challenges for the implementation of op-amps in deep submicron technologies. In addition, the op-amp must have high closed-loop bandwidth and settle fast. The non-dominant poles must be pushed out to high frequencies to achieve high bandwidth and stability simultaneously. These requirements make op-amp based circuits power inefficient. Moreover, technology scaling makes the realization of op-amps more difficult due to

reduced signal swing and intrinsic device gain. Cascoded amplifier stages have been a popular solution to increase amplifier gain, but they further reduce the signal swing. Special high gain devices have been developed to achieve high intrinsic gain for a power efficient op-amp based pipeline ADC [3]. However, such devices require additional processing steps to standard CMOS technologies.

It has been speculated that because of these issues it will be both economically and technically impossible to implement high resolution circuits such as data converters in low-voltage, deeply scaled technologies and that the optimality of "System on Chip" (SoC) integration may be ending in favor of "System in Package" (SiP) solutions, where functionality from different die are assembled in a single package [1]. The issues associated with taking signals "off-chip," however, greatly limit this approach, especially at higher speeds and resolutions.

Digital correction and calibration is an area that is providing methods of dealing with the issues of technology scaling. Digital calibration has been applied to a wide variety of ADC architectures including open-loop amplification [4], incomplete settling [5], low-gain closed-loop amplification [6], [7], and capacitive charge pump [8]. These techniques trade the robustness and accuracy the op-amp provides with lower power operation. The accuracy is recovered by often-times sophisticated digital calibration.

Another approach to deal with device and voltage scaling is an alternative architecture called Zero-Crossing Based Circuits (ZCBC) [9]–[12]. This architecture replaces the function of the op-amp with the combination of a comparator and current source to realize the same charge transfer as an op-amp based implementation. It completely eliminates op-amps from the design and does not require stabilizing a high-gain, high-speed feedback loop. This not only reduces complexity but also eliminates the associated stability versus bandwidth/power trade off while mostly retaining the robustness the op-amp provides.

This work further improves the resolution, power efficiency, and robustness of the previous ZCBC designs through various means including fully differential signaling, offset compensation, and output range enhancement. This paper is organized as follows: Section II introduces the fully differential ZCBC architecture used in this design. Section III describes the Chopper Offset Estimation technique developed for offset compensation. Sections IV and V cover the additional implementation details of reference voltage switching and output range enhancement via redundancy. Section VI covers higher level details and shows the complete ZCBC pipeline stage schematic. Section VII reviews the sub-ADC implementation. Section VIII provides the measured results, and Section IX concludes.
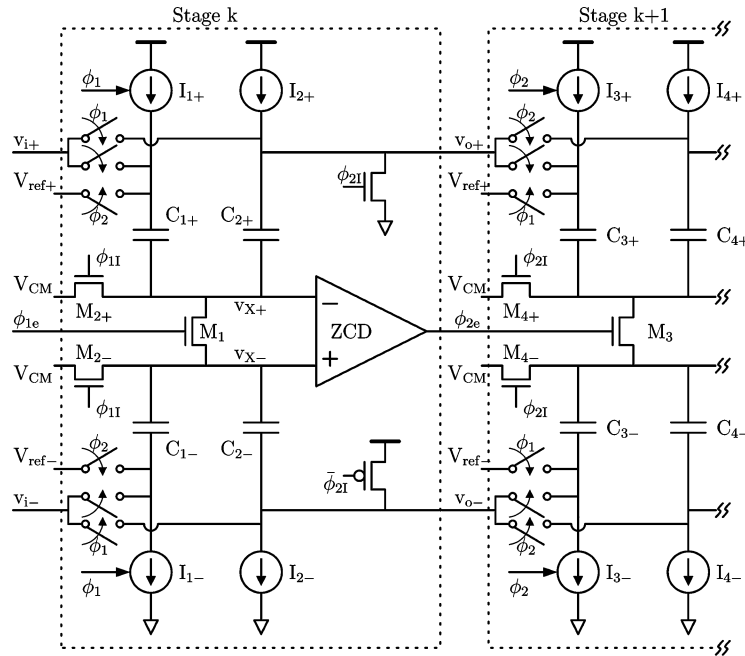
Fig. 1.   Simplified schematic of adjacent fully differential ZCBC pipeline stages.

II. Fully Differential ZCBC

When compared to its single-ended counterpart, a fully differential circuit implementation typically doubles the signal amplitude without affecting the noise level. Thus, the SNR of a fully differential circuit is 2 times that of its single-ended counterpart. Since the Figure of Merit (FOM) improves by the ratio of the increase in SNR to the increase in power consumption, a fully differential design can realize an improved FOM by up to a factor of 2 depending on the additional power consumed by the added differential circuitry, such as the common-mode feedback circuit. Therefore, coupled with the opportunities for better power supply and substrate noise rejection, this design uses a fully differential implementation of a ZCBC pipelined ADC.

A simplified schematic of two fully differential ZCBC pipeline stages is shown in Fig. 1. The corresponding timing diagram is shown in Fig. 2. When ϕ_1 is high and stage k is in the sampling phase, the input is sampled on capacitors $C_{1\pm}$ and $C_{2\pm}$. When ϕ_2 goes high and stage k enters the transfer phase, stage $k + 1$ enters the sampling phase and capacitors $C_{3\pm}$ and $C_{4\pm}$ become the load of stage k. During the transfer phase, all the charge on $C_{1\pm}$ is transferred to $C_{2\pm}$ to realize the desired voltage gain on the output. The differential zero-crossing detector (ZCD) must detect the virtual ground condition $(v_{x+} = v_{x-})$ as the current sources sweep the output over the output range.

The output voltage sweep begins with a short pre-charge phase when ϕ_{2I} goes high and the positive output node v_{o+} is initialized to ground and the negative output node v_{o-} is initialized to V_{DD}. This sets output below the minimum output range and provides a common mode reset of the output voltage. The inside plates of the output load capacitors $C_{3\pm}$ and $C_{4\pm}$ are also initialized during this pre-charge phase to the common mode voltage V_{CM}.

After the pre-charge phase, the current sources begin the sweep of the output voltage as they charge the capacitors to produce a linear voltage ramp. The positive channel ramps up while the negative channel ramps down. As in [10], each capacitor is charged with an independent current source to avoid the non-linearity introduced when charging through a series switch. Observe that switches $M_{4\pm}$ open after the pre-charge phase and switch M_3 is left closed to connect the inside plates of the load capacitors. The output of the zero-crossing detector switches when it detects the virtual ground condition. This opens switch M_3 to lock the charge on $C_{3\pm}$ and $C_{4\pm}$ and realize the desired charge transfer. M_3, therefore, is the sampling switch for the differential signal. It ties the inside plates together but allows the voltage on that node to float while the outputs are ramping. Letting the inside plates float together rather than leaving them connected to V_{CM} provides two advantages. First is that the resistance of the sampling switch is effectively halved, thus halving the voltage drop that reduces the range of the output signal. Second is that it ensures the positive channel capacitors (C_{3+} and C_{4+}) charge at the same rate as the negative channel capacitors (C_{3-} and C_{4-}) regardless of any current mismatch in the current sources. Thus, no common mode *charge* error accumulates while the output is ramping even if common mode error occurs on the output *voltage*. This means that when sampling is complete and the capacitors enter the pre-charge phase that the common mode voltage into the zero-crossing detector also gets reset as well.

A. Common Mode Control

A continuous time common mode feedback circuit is essential in a traditional fully differential op-amp based implementations. The reason is that the common mode of the output voltage of a fully differential op-amp is a function of both the differential and common mode of the input signal. In the case of a
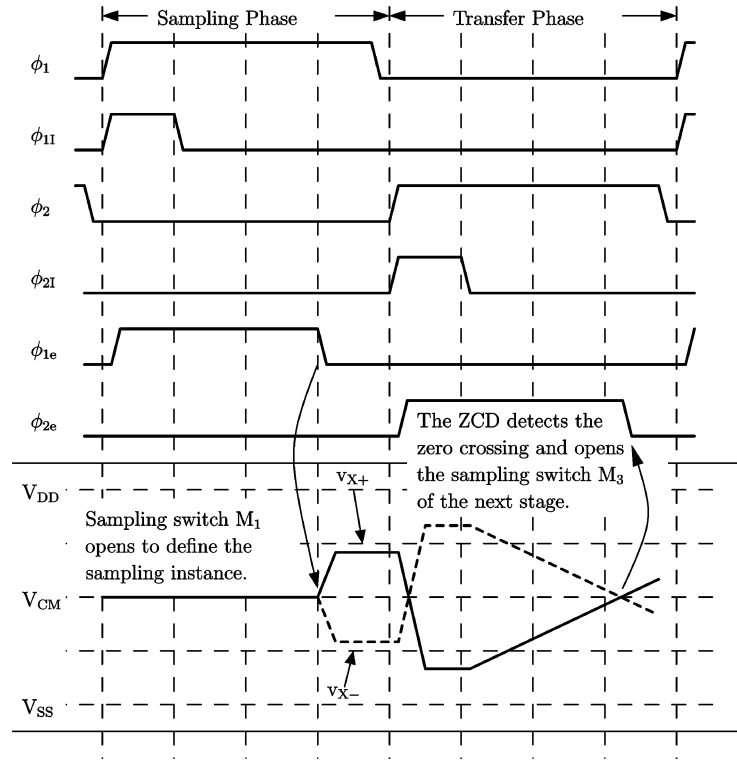
Fig. 2. Timing diagram for fully differential ZCBC implementation.

ZCBC implementation, however, the output voltage common mode is set by the relative strengths of positive and negative current sources and does not depend on the common mode performance of the zero-crossing detector. Any mismatch in relative strength of the positive and negative current sources is absorbed by the reference-side capacitors ($C_1\pm$ and $C_2\pm$) and produces a small output voltage common mode error that grows with the voltage ramp. Coupled with the fact that the common mode error gets reset both on the ouput and on the input into the ZCD after the ramping is complete, a common mode feedback circuit was found unnecessary for this ZCBC implementation.

B. Symmetry for Improved Power Supply Noise Rejection

Fully differential implementations typically have good power supply noise rejection due to circuit symmetry between the positive and negative signal channels. In a symmetric implementation, power supply noise affects both channels equally to first order and thus only affects the common mode signal and not the differential signal.

One source of asymmetry obvious in the simplified schematic of Fig. 1 is the current source polarity. The positive channel has pMOS based current sources connected to V_{DD} and the negative channel has nMOS based current sources connected to ground. Large and small signal schematics of the positive channel output node with a pMOS based current source (M_5) are shown in Fig. 3. In the small signal model, the voltage source represents the power supply noise, r_o is the output impedance of the current source, C_{db} is the parasitic drain-to-bulk junction capacitance of the current source, and r_{on} is the series resistance of the sampling switch M_3.
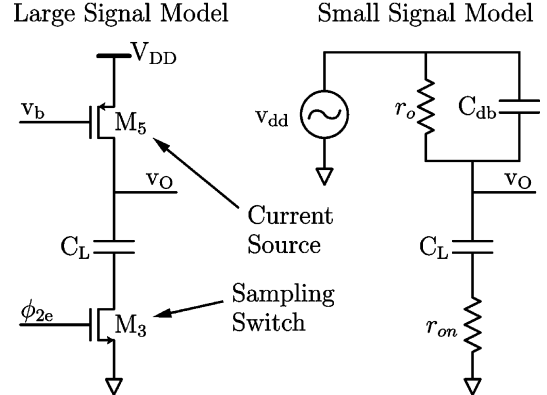

Fig. 3. Large and small signal schematics of pipeline stage output node for power supply noise analysis.

The voltage transfer function from the power supply to the output node under the assumptions that $C_L \gg C_{\text{db}}$ and $r_o \gg r_{\text{on}}$ is

$$\frac{v_O(s)}{v_{dd}(s)} \approx \frac{sr_oC_{\text{db}} + 1}{(sr_oC_L + 1)(sr_{\text{on}}C_{\text{db}} + 1)}. \quad (1)$$

This is plotted in Fig. 4 for parameters extracted from this design. For low frequencies the power supply noise feeds directly to the output with unity gain. The first pole occurs at $1/r_oC_L$ when the impedance of C_L becomes active. Even if noise disturbs the voltage ramp, as long as the ZCD switches to open the sampling switch when the inputs cross, the correct voltage will be sampled on the output capacitors. The bandwidth of the
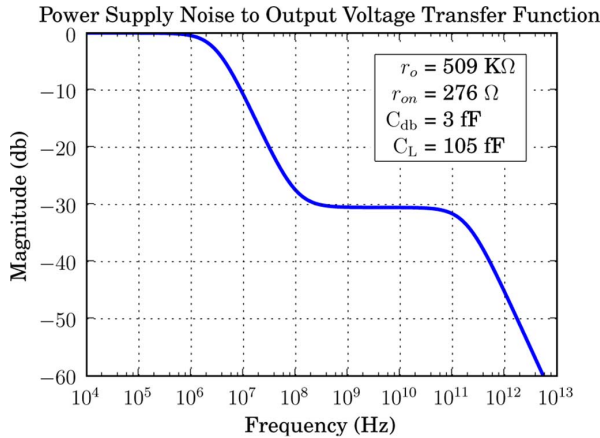
Fig. 4. Power supply to output voltage transfer function from parameters extracted via simulation.

Fig. 5. Permanently disabled current sources $I_{\mathrm{dum}}\pm$ are added to provide symmetric parasitic capacitance for improved power supply noise rejection.

Fig. 6. Differential zero crossing detector with digitally programmable offset adjustment.

ZCD in this design is sufficient to track and null the low frequency power supply noise, but the more problematic power supply noise occurs at higher frequencies when the frequency response flattens for about three orders of magnitude due to the zero at $1/r_o C_{\mathrm{db}}$. High frequency noise faster than than the ZCD response can be sampled into the output capacitors when the ZCD is unable to switch at the precise time when the inputs cross.

The zero in the power supply transfer function is caused by the parasitic junction capacitance C_{db} and since it is above the bandwidth of the zero-crossing detector, it will be sampled at the output. Minimizing the capacitance ratio of C_{db} to C_L maximizes the attenuation of the high frequency power supply noise, but this comes at the expense of signal range as reducing the width of the current source device raises its required drain-to-source voltage.

Another approach to effectively eliminate the high frequency power supply noise is to exploit symmetry by putting the same parasitic junction capacitance on both channels of the fully differential signal path. In this case, the power supply noise will feed equivalently (to first order) into both channels and appear as a common mode voltage error. To load the output node equivalently in the implementation, dummy current sources were added to each channel as shown in the partial circuit diagram of Fig. 5. Since these current sources are permanently disabled, the added parasitic capacitance only increases the dynamic power consumption slightly.

C. Differential Zero-Crossing Detector

A fully differential ZCBC requires a differential zero crossing detector. The dynamic zero-crossing detector (DZCD) used in [10] is power efficient but inherently single-ended and does not have a natural extension to a differential implementation. The differential zero-crossing detector shown in Fig. 6 is used in this implementation. The first stage is a differential to single-ended pre-amplifier followed by a dynamic threshold detecting latch (DTDL).

The pre-amplifier is implemented with an nMOS differential pair (M_1 and M_2) input. A current mirror (M_3 and M_4) is used to convert from a differential signal to a single-ended output.
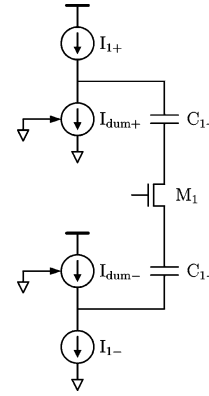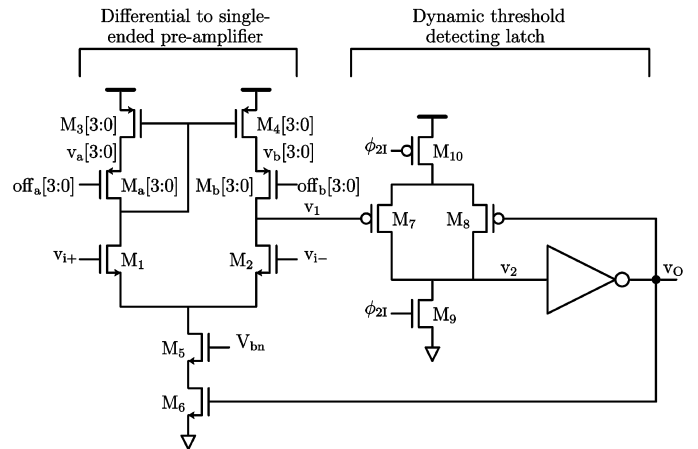
Devices M_3, M_4, M_a and M_b utilize iterated instance notation to reprasent 4 devices placed in parallel. Nets $v_a[3:0]$ and $v_b[3:0]$ use bus notation to represent 4 different nets hooked up to the individual iterative device instances. Devices M_3, M_4, M_a, and M_b have binary weighted widths to create a programmable current gain by enabling or disabling devices M_a and M_b independently. This programmable current gain creates an offset programmable pre-amplifier that is used for offset compensation. The measured programmable offset range is plotted in Fig. 7 and is discussed further in Section III. This pre-amplifier implementation preserves the power supply rejection of the fully differential design as the single-ended conversion occurs after the gain of the amplifier.

The DTDL is composed of devices M_7–M_{10} and is like the dynamic ZCD used in [10] in that it is a dynamic logic circuit that draws no static current. During the pre-charge phase with ϕ_{2I} high, the latch is reset when M_{10} turns off and M_9 turns on. In this state, the tail current to the pre-amplifier is turned on via switch M_6. When ϕ_{2I} drops to enter the transfer phase, voltage v_1 begins to drop. The zero-crossing is detected when the virtual ground condition has been reached ($v_{i+} = v_{i-}$) and v_1 drops sufficiently to flip the state of the latch. At this point the bias current of the pre-amplifier is shut-off by disabling device M_6. Thus, while the pre-amplifier draws static current prior to the
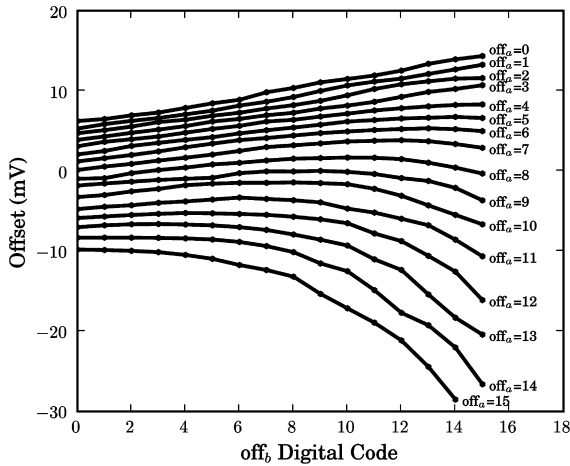
Fig. 7. Measured first stage programmable ZCD offset range. See Fig. 6 for definition of off_a and off_b nets.
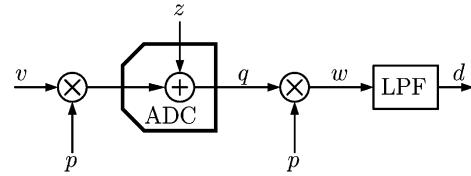

Fig. 8. Traditional chopper stabilization for offset compensation.
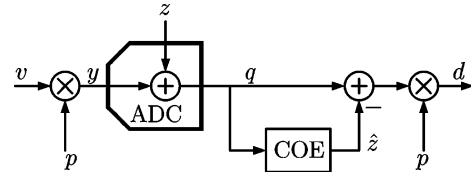

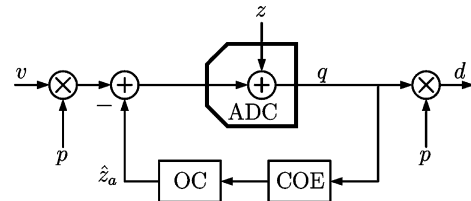Fig. 9. Alternate chopping technique utilizing a chopper offset estimation (COE) block.

Fig. 10. Block diagram using chopper offset estimation (COE) and offset controller (OC) blocks to null the ADC offset in the analog domain.

threshold detection, the current is turned off after the detection to save power.

III. CHOPPER OFFSET ESTIMATION

As flicker noise increases [13] and signal range decreases with technology scaling, offset compensation is becoming increasingly important for analog circuit design in general. Offset compensation is also important specifically to ZCBCs to increasing their robustness to variation in parameters such as temperature and ramp rate. Traditional closed-loop offset compensation techniques, however, are not compatible with ZCBCs because they can not drive both sides of the sampling capacitor simultaneously and because the offset of concern in a ZCBC is its dynamic offset, which is not necessarily equal to the static offset measured via closed-loop techniques.

Chopper stabilization (CHS) [14]–[16], on the other hand, is a traditional technique compatible with both traditional opamp-based and ZCBCs. It is indiscriminate to the sources of offset and is not susceptible to second order circuit issues such as charge injection or finite open-loop gain. One large disadvantage of CHS is that it requires high performance filtering to remove the offset, and such filtering can be area and power intensive. To overcome this issue, a derivative technique called Chopper offset estimation (COE) is used in this design that retains the advantages of CHS but reduces the filtering requirements and can also recover the lost signal range due to offset.

A. Traditional Chopper Stabilization

A block diagram of traditional CHS for an ADC application is shown in Fig. 8. The analog input voltage v is modulated by a chopping vector p prior to quantization by the ADC. The vector p is a tone at $f_s/2$, where f_s is the sampling frequency. It takes the form $p = [+1, -1, +1, -1, \ldots]$. This modulation shifts the input signal up in frequency to $f_s/2$. After modulation, the signal is quantized by the ADC. The ADC adds an unknown offset z while generating the digital output q. The offset is assumed to be low in frequency and is therefore added out of band of the input signal that has been frequency shifted up.

After quantization, q is digitally demodulated by the same chopping vector p to frequency shift the input signal back down and shift the offset up to $f_s/2$. A wideband low-pass filtered (LPF) is then used to filter away the offset while preserving the signal.

For a fully differential design, modulation by the vector p can be implemented with two extra switches that switch the input polarity as appropriate [15]. The demodulation of the ADC output is also a simple matter of digitally inverting the appropriate samples. The low pass filter, on the other hand, introduces a significant trade-off between hardware complexity and adequate frequency response. The LPF must be able to meet the frequency response requirements of the application in terms of transition band steepness, pass-band ripple, phase response, and latency while also trying to limit the extra sampling bandwidth requirement.

B. Chopper Offset Estimation (COE)

Chopper offset estimation (COE) as shown in Fig. 9 can be used to reduce the filtering requirements of traditional CHS and can be obtained through simple manipulations to the block diagram in Fig. 8. The basic concept is to use a COE block to estimate the low frequency offset added by the ADC immediately after quantization so that offset estimate can be subtracted from the signal prior to demodulation.

This modification offers the possibility for significant hardware savings in the low-pass filter. Traditional CHS must implement a wideband low-pass filter that removes the offset and must run at the full sampling rate. The COE LPF, however, must implement a narrow band filter to estimate the offset and can run at a much lower rate. This advantage was realized in the ADC
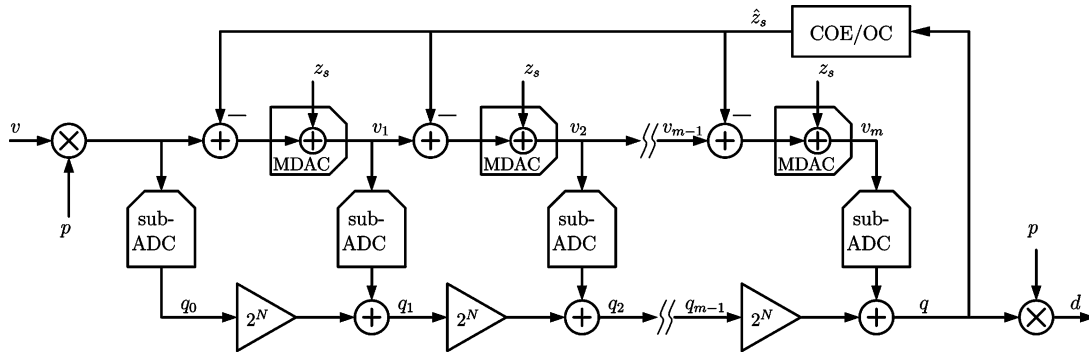
Fig. 11. Block diagram of an m stage pipelined ADC with identical COE offset correction distributed to each pipeline stage.

implementation in [17] where a tunable single pole infinite impulse response (IIR) filter was used to implement the COE filter. While this approach is simple, it causes the frequency response of the ADC to have non-linear phase and ripple in the pass band. An alternative approach that can realize similar hardware savings with linear phase and more controlled pass band ripple is to employ polyphase decimation finite impulse response (FIR) filters [18] that sub-sample the offset estimate. This can realize hardware savings on the order of the ratio of the bandwidth of the offset to the bandwidth of the signal, which can be many orders of magnitude in many applications.

C. Input Referred Offset Compensation With COE

One additional disadvantage of traditional CHS is that the offset is not removed in the analog domain, so the offset reduces the available signal range. Since the COE block, however, produces a digital offset estimate $\hat{z}$, an alternative offset correction scheme is to pass the offset estimate to an offset controller (OC) to null the offset at the source in an input-referred fashion as shown in Fig. 10.

An input referred COE approach was applied to a two-step ADC architecture in [19]. When using this technique with a pipelined ADC, however, it is critical that the offset correction be injected at the appropriate spot in the analog processing chain if one desires to recover the signal range that is lost due to the offset. Because ZCBC pipelined ADCs are dominated by systematic offset caused by overshoot due to the finite delay of the zero-crossing detector, this implementation distributed the same offset correction factor to the input of each stage as shown in the block diagram of Fig. 11. This technique cancels both the systematic and random offset with minimal complexity. The OC is a simple band selection and up/down counter that digitally controls the offset curves shown in Fig. 7 to null the digitally measured offset $\hat{z}$.

A more in depth look at additional chopping architectures specifically for ZCBC's can be found in [12]. This source also includes discussion on the tradeoffs of using a random chopping vector that is uncorrelated to the input for applications where the full bandwidth of the signal is required and the offset cannot be injected out of band.

IV. VOLTAGE REFERENCE SWITCHING

During the transfer phase an analog multiplexer must switch between the reference voltages based on the bit decisions of the
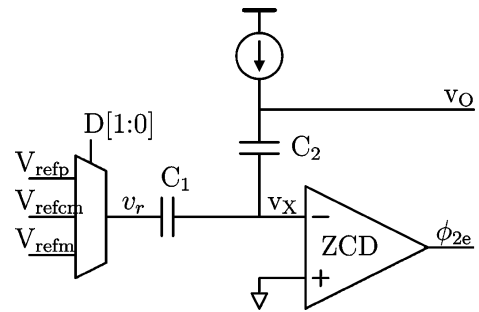

Fig. 12. Traditional implementation of voltage references for a 1.5 bit/stage pipeline stage.

sub-ADC. In an op-amp based circuit, the current through these switches decays as the dynamics settle. In a ZCBC implementation, however, the current is constant for the entire ramping period, and the series ON-resistance of these switches introduces a voltage drop. The voltage drop in the reference switches for a 1.0 bit/stage case is not an issue because two reference points are inherently linear even if the drop for the high reference is different than the low reference. When additional reference points are introduced, however, a non-linearity will result if the drop across each resistor is not the same.

A 1.5 bit/stage design with three reference levels like that shown in the schematic of Fig. 12 was used in [10]. That design used gate-boosted switches for the reference voltage to generate switches with matched ON-resistance to meet the linearity requirement (see (3)). For this design, however, a switch capacitor technique is used to generate the middle voltage reference to reduce the number of references to two and eliminate the series ON-resistance as a linearity issue. The schematic for this approach is shown in Fig. 13. Capacitor C_1 has been split in half and is driven with two reference voltage multiplexers that can interpolate the middle voltage as necessary. Thus, when the bit decisions $D[1:0]$ require driving either V_{refp} or V_{refm}, both analog multiplexers drive the corresponding voltages. When the third V_{refcm} voltage is required, one multiplexer drives to V_{refp} and the other to V_{refm} to interpolate the middle reference voltage. As shown in Appendix A, the response will be linear even if ON-resistance of the switches is different. This method, however, does require capacitor C_1 to split in half accurately. Implementing matched capacitors is much more prac-
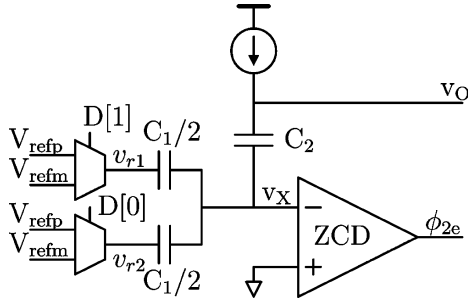
Fig. 13. Alternative 1.5 bit/stage ZCBC implementation where C_1 has been split to eliminate the V_{refcm} voltage reference and avoid linearity issues from switch resistance.
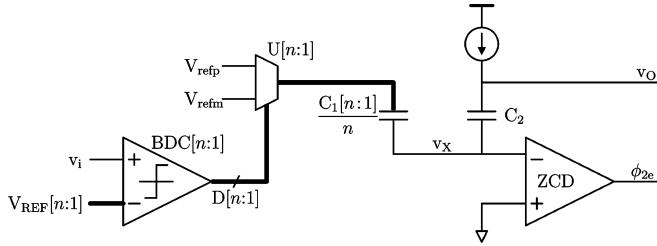

Fig. 14. Schematic of a $\log_2(n+1)$ bit/stage ZCBC pipeline stage using capacitor splitting (only circuits active during the transfer phase have been included). Capacitor C_1 is split into n equal parts.
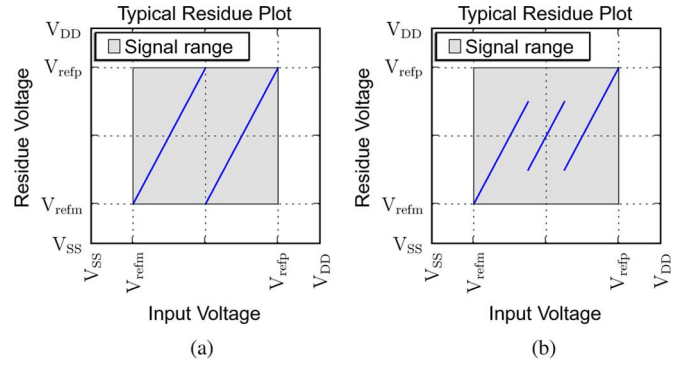

Fig. 15. Typical residue plots without redundancy and with redundancy.

Fig. 16. Residue plots when using 2 bit decision comparators (1.58 bits/stage).

tical than generating switches with a constant ON-resistance at different voltage levels.

This technique has a natural extension to higher resolutions. The rule is that capacitor C_1 should be split up equally to match the exact number of bit decision comparators in the sub-ADC and each bit decision comparator controls the select logic for the multiplexer for each capacitor directly. The single-ended schematic of a ZCBC stage in the transfer phase in Fig. 14 shows such an implementation for the case of when n bit decision comparators are used to create a $\log_2(n+1)$ bit/stage pipeline stage. This schematic uses iterative instance notation to denote multiple parallel instances and thick line to denote buses of multiple nets. The thermometer encoded output $D[n:1]$ of the bit decision comparators $BDC[n:1]$ drives the select of the multiplexer $U[n:1]$ directly.

Appendix A analyzes the fully differential case and can be summarized with two statements. First, the series voltage drop Δ due to the ON-resistance of the reference voltage switches adds an offset to the residue output. This offset gets added to all the other sources of offset and is nulled by offset compensation. Second, even though the drop across the switches will reduce the available signal range, the response is linear to within the matching of split capacitors even if the V_{refp} switch drop is different than the V_{refm} drop.

V. REDUNDANCY FOR INCREASED SIGNAL RANGE

Redundancy or over-range protection is traditionally used to relax offset constraints in both the bit decision comparators and the residue amplification [20]. A typical residue plot with and without redundancy is plotted in Fig. 15. The gray area represents valid signal area, and adding extra bit decisions to create redundancy helps protect the signal from leaving the valid signal
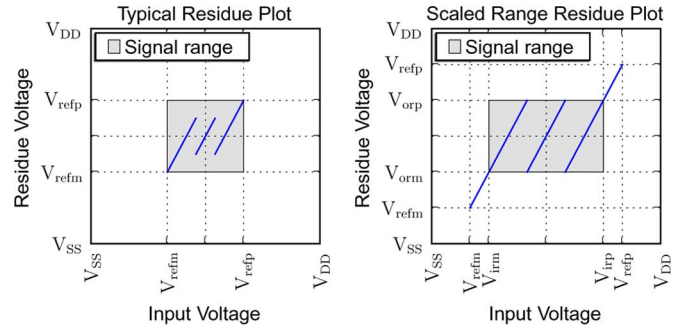
area in the presence of bit decision comparator offset or residue amplification offset.

Since the output signal range matches the input signal range both with and without redundancy, the gray shaded area that highlights the valid signal range is square in both cases. Even though redundancy does reduce the output range at the bit decision boundaries, the extreme edges of the input near V_{refp} and V_{vrefm} still swing over the complete range. Therefore, the output linearity of the residue amplification stage must be designed to match the input range.

When designing in scaled technologies, however, the output range of the residue amplifier can be extremely limited, especially if cascoded devices are used in the output stage. The input range, on the other hand, in many cases may not be so limited, especially if passive sampling is used. If the output range is limited, as shown in the example of the first plot of Fig. 16, traditionally the input range must also be reduced to match it. An alternative approach, however, is to grow the reference voltages until the output range of the interior step transition points reaches the maximum output range. This, of course, grows the input range at the same rate and produce regions where the output goes out of range. Shrinking the input range (V_{irm} to V_{irp}) via a policy change without changing the reference levels, however, can eliminate these invalid regions by removing the tails of residue plot so that the input range is larger than the required output range. This is the technique used in the second plot of Fig. 16. The gray box representing the valid signal range is no longer square but rectangular as the input range is larger than the output range. Furthermore, comparing both plots of Fig. 16 shows that the output range of both residue plots is identical,
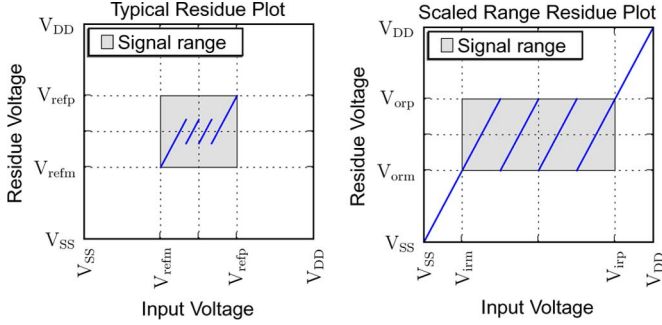
Fig. 17. Residue plots when using 3 bit decision comparators (2.0 bits/stage).
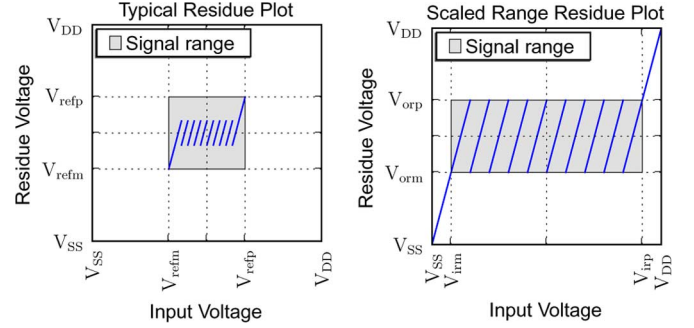

Fig. 18. Residue Plots for gain $G = 4$ and number of bit decision comparators $n = 9$. This yields a 3.3 bit/stage pipeline ADC with gain reduction.

but the input range of the left-side plot is larger. In this example it has grown by a factor of 1.5 for the same output range. This change does not require changing anything in the circuit other than to increase the reference voltages V_{refm} and V_{refp} the appropriate amount. Thus, since the noise level and the power consumption stay the same while the signal range increases, the SNR and power efficiency improve. For the example of Fig. 16, the reference voltages have been scaled by a factor of 2 to realize an increase of 1.5 in input range for the same output range, which amounts to an increase in SNR^2 of 2.25.

Further redundancy can be employed to allow for further reference voltage scaling. This can be seen by comparing the residue plots of Fig. 16 to Fig. 17. Fig. 16 corresponds to a stage with 2 bit decision comparators that implement a 1.5 bit/stage pipelined ADC. Fig. 17, on the other hand, corresponds to a stage with 3 bit decision comparators, or 2 bits/stage. Both have the same output range, but the later has a larger input range. In this case the reference voltages were scaled by 3 to realize a 2 times larger input range, which corresponds to a 4 times improvement in SNR. Adding additional redundancy for further improvements in this example would require scaling the reference voltages beyond the power supply range, which is impractical for most applications. One side benefit that is also realized by using reference voltage scaling is that as the reference voltages push closer to the power supply it eases the switch sizing requirements that realize the analog multiplexer described in Section IV.

The problem with using reference voltage scaling as introduced to this point is that the over-range protection to bit decision comparators and zero-crossing detector offset has been reduced to nothing. Thus, when defining the available output range, one must include margin for all sources of offset that can affect the residue plot. For example, suppose a given process has a 1.2 V supply and that V_{dsat} is 175 mV. If cascoded current sources are used, then $2\,V_{\text{dsat}}$ must be removed from both sides of the power supply to reduce the available output range to 0.5 V. Suppose further that the zero-crossing detector offset is nulled, and that the input referred BDC offset is $\pm 25\,\text{mV}$ worst case. Then the output referred offset will be $\pm 50\,\text{mV}$. Taking 50 mV away from both sides of the available output range reduces it to 0.4 V. The typical implementation would then set $V_{\text{refp}} = 0.8\,\text{V}$ and $V_{\text{refm}} = 0.4\,\text{V}$ and limit the input range to 0.4 V to match the available output range. Using reference voltage scaling, on the other hand, with a redundancy of 3 bit

decision comparators allows for the reference voltages to scaled by a factor of 3 so that the $V_{\text{refp}} = 1.2\,\text{V}$ and $V_{\text{refm}} = 0\,\text{V}$. The input range would then scale by a factor of 2 to 0.8 V, and the SNR^2 would increase by a factor of 4. These are the same conditions that plotted in the residue plots of Fig. 17.

Voltage reference scaling can be generalized for the case when n bit decision comparators are used to realize a $\log_2(n+1)$ bits/stage pipeline stage and when the residue amplifier gain is G. The case of no redundancy is when $\log_2(n + 1) = G$ and redundancy is introduced whenever $\log_2(n + 1) > G$. As compared to the case when no redundancy is used, using redundancy can increase the input range by a factor

$$ x_{ir} = \frac{n + 1}{G} $$

when the reference voltages are scaled by a factor

$$ x_{\text{ref}} = \frac{n}{G - 1}. $$

The SNR^2 then scales as the square of the input range, so the

$$ x_{\text{SNR}} = \left(\frac{n + 1}{G} \right)^2. $$

In the example shown in Fig. 16, $G = 2$ and $n = 2$, and the input range scales by a factor of 1.5, the reference voltages scale by a factor of 2, and the SNR^2 by 2.25. In the example shown in Fig. 17, $G = 2$ and $n = 3$.

For this design, the maximum V_{DD} is 1.2 V. With a V_{dsat} of 150 mV and input referred BDC offset of 25 mV, the available output range is 0.4 V. By selecting $G = 4$ and $n = 9$, the input voltage range can scale by a factor of 2.5 from 0.4 V to 1.0 V, the references scale by a factor of 3 from 400 mV to 1.2 V, and the SNR^2 scales by a factor of 6.25. The residue plots both without and with reference voltage scaling for this particular case are shown in Fig. 18.

VI. COMPLETE ZCBC PIPELINE STAGE

The schematic of a complete pipeline stage implemented for this fully differential design is shown in Fig. 19. This schematic also uses iterative instantiation notation to represent devices placed in parallel and thick lines to represent buses. As shown, there are nine $C_1\pm$ capacitors and three $C_2\pm$ capacitors, which realizes a gain of 4. There are twelve unit capacitors driven
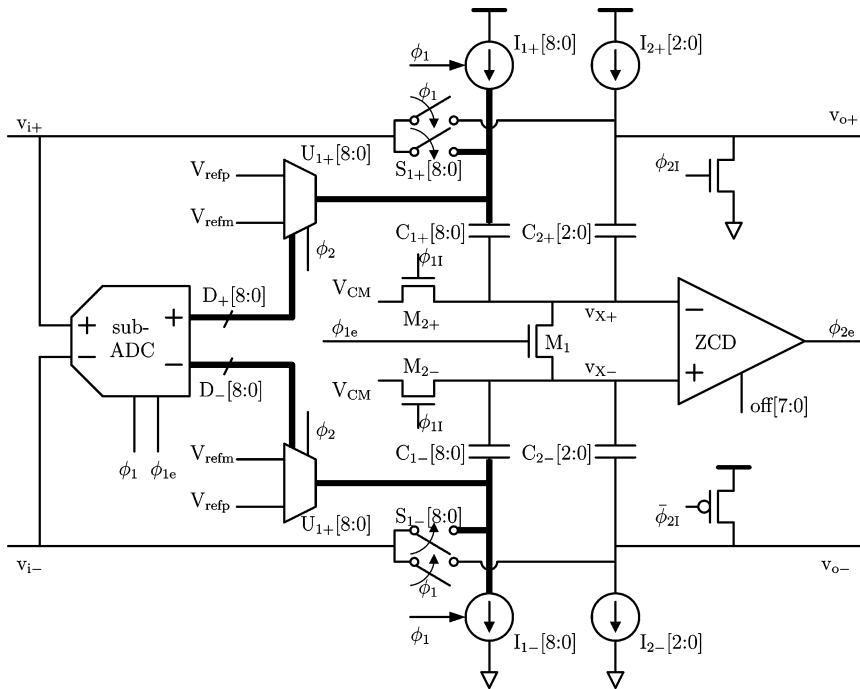
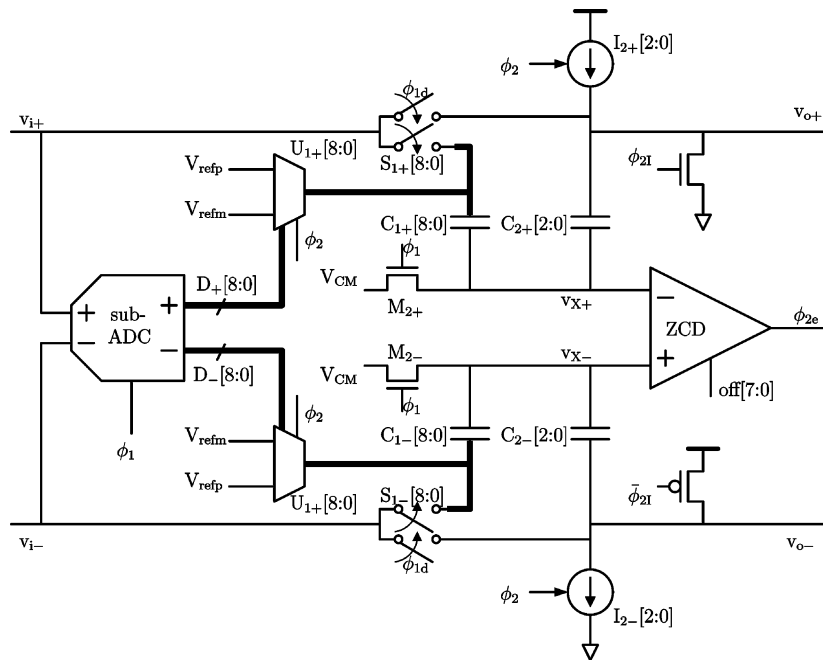Fig. 19. Complete ZCBC fully differential pipeline stage.

Fig. 20. First stage of ZCBC fully differential pipeline ADC.

with twelve current sources on each side. Not shown are the twelve dummy current sources for each side. The ten level (3.3b) sub-ADC includes nine bit decision comparators. The nine outputs of the sub-ADC differentially drive nine analog reference voltage multiplexers. The sampling switch M_1 is connected to the zero-crossing detector output of the previous stage. The offset of the zero-crossing detector is digitally programmed via the bus labelled off [7:0].

The first stage of the ZCBC pipelined ADC as shown in Fig. 20 is slightly different than other stages. Sampling device M_1 has been removed so that devices $M_{2\pm}$ sample the input with respect to the common mode voltage for the entire duration of the sampling phase. Since ϕ_1 falls prior to ϕ_{1d}, these switches open first to perform bottom-plate sampling. Because the sampling capacitors of the first stage sample the input voltage directly, these capacitors do not require current sources to generate voltage ramps during sampling. During the transfer phase, however, current source $I_{2\pm}$ generates the voltage ramp on the series connected sampling capacitors.
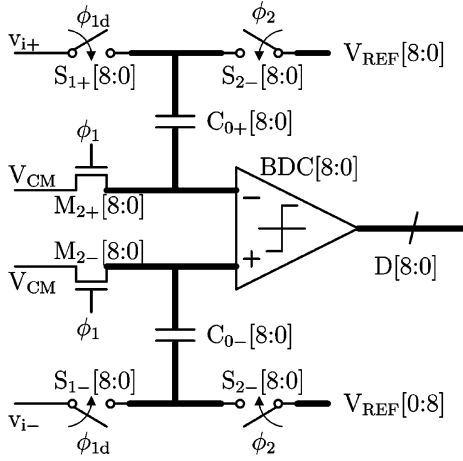
Fig. 21. First stage SUB-ADC implementation utilizing bottom plate sampling.

Fig. 22. SUB-ADC implementation for all stages except the first.

Although it is not shown in the first stage schematic of Fig. 19, the input sampling switches $S_{1\pm}$ are implemented as a switching matrix as introduced in [15] to allow for input chopping. Furthermore, these switches are boosted to produce a constant V_{gs} in the same way as [10]. Except for these four input sampling switches, this design uses no additional gate-boosted switches unlike design [10] which used gate boosting for the reference switches and current source shorting switches.

To realize a 12 bit ADC, six pipeline stages are implemented. The first stage is scaled four times larger than the remaining stages, which are identical. The unit capacitance of the 12 capacitors of the first stage is 415 fF, meaning the total input capacitance is approximately 5 pF on each input terminal.

VII. SUB-ADC DESIGN

A. Circuit Architecture

While over-range protection minimizes the impact of offsets in the sub-ADC of each stage, any offset increases the required output range. Therefore, in this design, special care was given to ensure that no systematic or frequency dependent offset was introduced into the sampling path of the sub-ADC of each stage.

Fig. 21 shows the sub-ADC used in the first stage. It matches the first stage sampling circuitry and timing. Bottom plate sampling [21] is used by turning off switches $M_{2\pm}$ prior to switches $S_{1\pm}$ to reduce signal dependant charge injection. After sampling completes when ϕ_1 falls, ϕ_2 rises to close switches $S_{2\pm}$. This subtracts and inverts the differential V_{REF} signal from the sampled input. The bit decision comparator is enabled a short time later to produce the bit decisions $D[8:0]$. The schematic of Fig. 21 uses iterative instantiation to show the parallel instantiation of the nine circuits that make up the sub-ADC. The nine different references voltages $V_{REF}[8:0]$ are generated using a resister string.

The sub-ADC for the stages that follow the first must also sample using the same circuitry as the signal path to avoid systematic offset in the bit decision locations. Fig. 22 shows the implementation. Just as the sub-ADC for the first stage, the
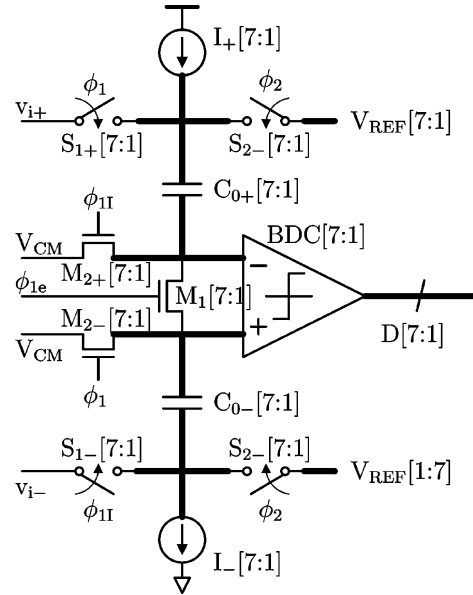
sub-ADC for the remaining stages uses switched capacitor techniques to subtract the reference voltage from the signal prior to comparison to generate the bit decisions $D[8:0]$.

The sub-ADC implementation for all the stages following the first do not implement the two outermost bits decisions and only utilize seven parallel circuits to generate the seven inner bit decisions. This is because the output range is reduced by a factor of 2.5 over the input range, and the output range of the the first stage becomes the input range of the next stage. Thus, the input into the stages after the first cannot be in the outermost bit decision range unless there are severe over-range issues. While more than just the two outermost bits can be dropped, each bit dropped reduces the over-range protection by the size of the bit decision quantum. These bit decisions cannot be dropped completely, however, because all nine bit decisions are required to drive the analog voltage reference selection multiplexer. Instead, the outermost bit decisions are simply hard-coded to eliminate the actual instantiation of a bit decision comparator to make a comparison. This saves a marginal amount power, area, and complexity.

B. Bit Decision Comparator Design

The initial mask set for this design contained the bit decision comparator (BDC) labelled as BDC A in Fig. 23. Devices M_3–M_6 make a cross coupled latch that is reset via devices M_7–M_{10} when the clock ϕ goes low. When the clock goes high, the comparator enters the evaluation phase which is controlled by the input pair M_1 and M_2. As can be see from the BDC A column of measured ADC results of Fig. 25, this BDC had so much offset and noise that the over-range protection was insufficient to keep the signal in range and the ADC has severe distortion.

This high offset and noise is due to the fact the input pair starts in the linear region when the enable devices M_9 and M_{10} turn on to start the comparison. When the enable devices turn on, however, they start in saturation and have much higher transconductance into the latch. Since the input-referred offset caused by
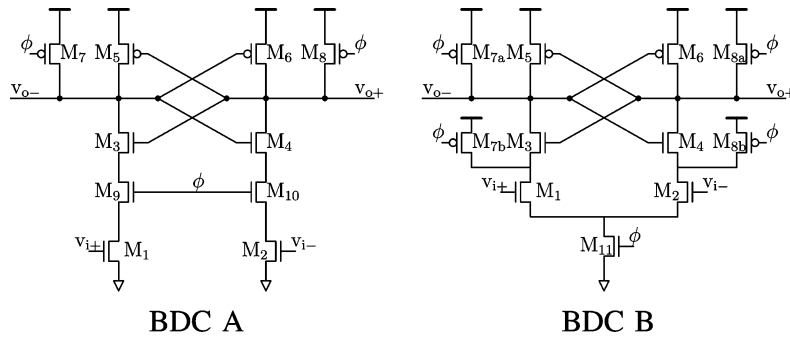
Fig. 23. Schematic of bit decision comparators (BDCs). BDC A was used initially and had offset and noise issues. BDC B was used via mask change to solve the problem.
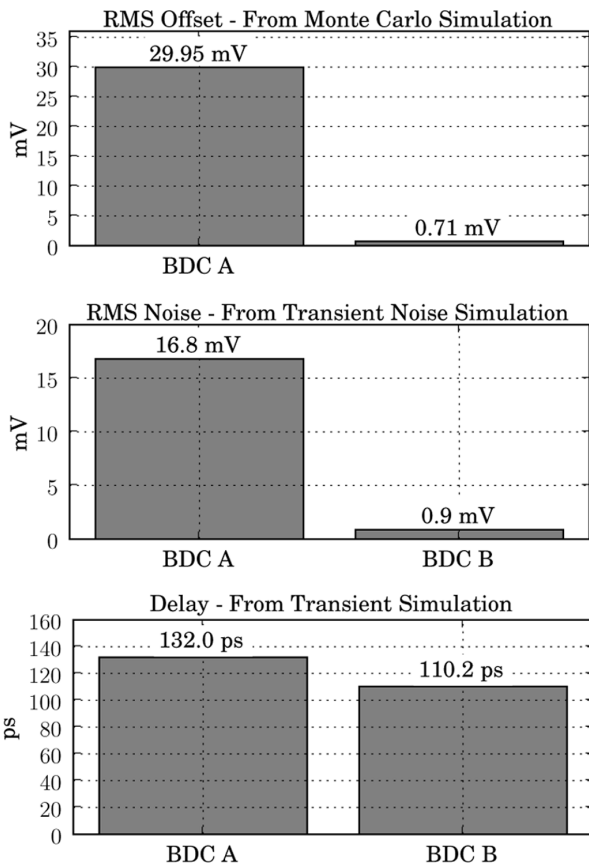

Fig. 24. BDC comparison simulation results.

Fig. 25. Measured ADC performance using BDC A and BDC B.

the enable devices gets amplified by the transconductance ratio of these devices, the input referred offset is large and dominated by the mismatch of the enable devices.

Through a mask change, however, the bit decision comparator was reconfigured as BDC B as shown in Fig. 23. This reconfiguration primarily involved swapping the position of the input pair and the nMOS enable switches. This allows the input pair to start the comparison in saturation to give it much more initial transconductance into the latch. As the Monte Carlo offset simulations in Fig. 24 show, BDC A has more than an order of magnitude more RMS offset than BDC B. As also shown in the simulation results of Fig. 24, BDC A is also noisier and
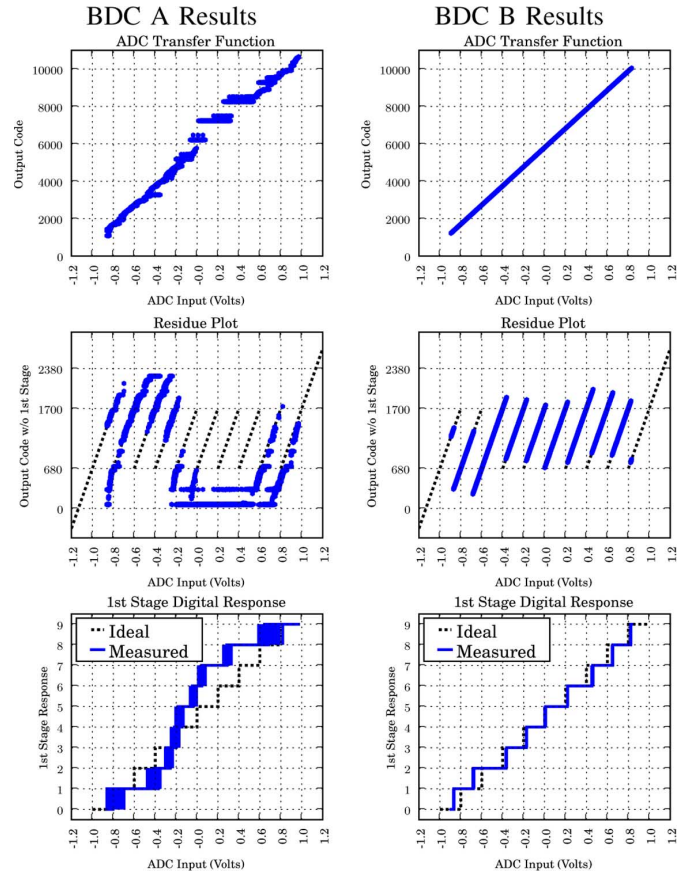
slower for the same reason that the input devices have much less transconductance into the latch at the start of the comparison.

While the measured results of BDC B did not provide the full order of magnitude improvement that the Monte Carlo simulations predicted, the offset and noise is improved sufficiently to keep the signal in range and for the ADC to reach the later stated performance. The offset of the BDC, however, is still larger than the margin allocated and is what limits the linearity of the ADC as it requires the voltage ramp to have a larger output range than planned for the cascoded current sources. This is believed to be the major limiting factor in the INL and ENOB as described in Section VIII.
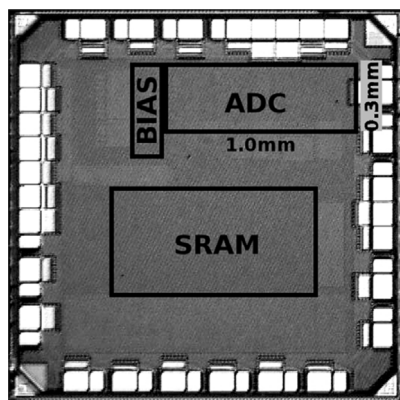
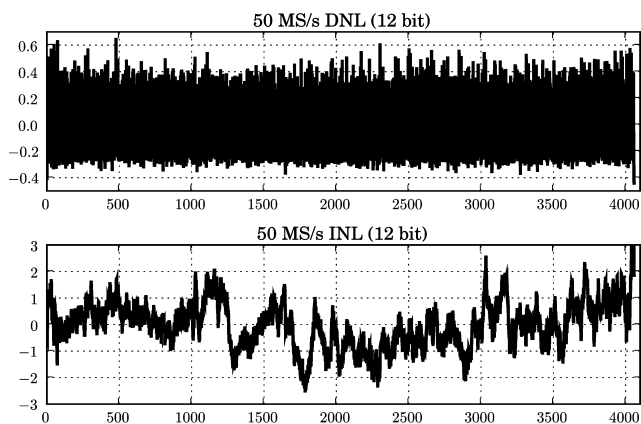Fig. 26.   Die photo of fully differential ZCBC ADC in 90 nm CMOS.
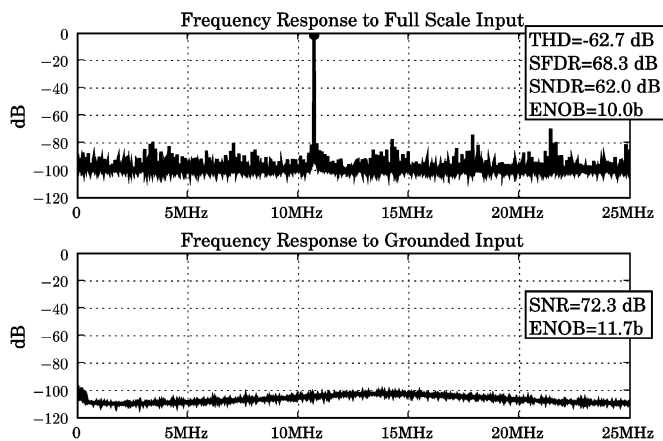

Fig. 27.   Measured linearity.

Fig. 28.   Measured frequency response.

Fig. 29.   SNDR, SFDR, and dynamic range versus sampling frequency.
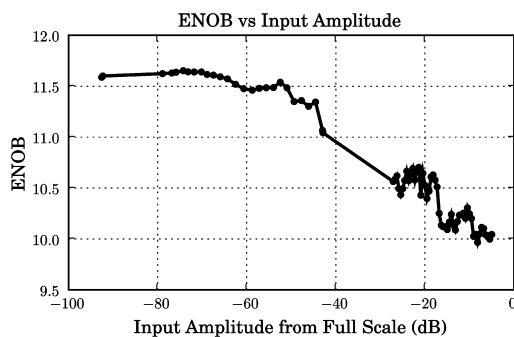
Fig. 30.   ENOB versus input amplitude.

TABLE I
ADC PERFORMANCE SUMMARY

Technology	90nm CMOS	
Area	$0.3\ \mathrm{mm^2}$	
Input Voltage Range	2V (differential)	
Power Supply: V_{DD}	1.2V	
Sampling Frequency	25 MS/s	50 MS/s
DNL	$\pm 0.5\ \mathrm{LSB_{12}}$	$\pm 0.5\ \mathrm{LSB_{12}}$
INL	$\pm 2.0\ \mathrm{LSB_{12}}$	$\pm 3.0\ \mathrm{LSB_{12}}$
Power Consumption	3.8 mW	4.5 mW
Dynamic Range	72 dB	72 dB
SFDR	73 dB	68 dB
SNDR	66 dB	62 dB
ENOB	10.6 bit	10 bit
Figure of Merit: $\dfrac{P}{2f_{\mathrm{in}}2^{\mathrm{ENOB}}}$	98 fJ/step	88 fJ/step

VIII. MEASURED RESULTS

The die photo for this design as implemented in a 90 nm CMOS process is shown in Fig. 26. The ADC uses an active area of $0.3\ \mathrm{mm^2}$. At 50 MS/s, the power consumption from a 1.2 V supply is 4.5 mW. This power consumption measurement includes power consumed by the references, bias circuits, and core digital logic. It does not include ancillary digital circuitry such as the SRAM and I/O drivers. The reference voltages are set to V_{DD} and ground to give an full scale input range of 2 volts. As shown in the linearity plots of Fig. 27, the DNL and INL are
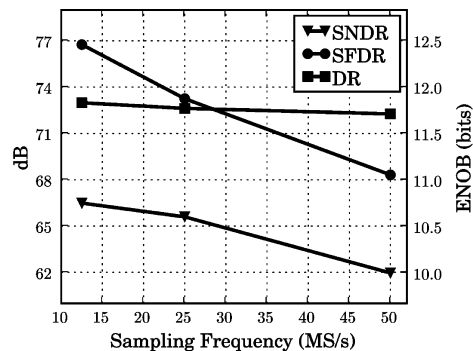
± 0.5 LSBs and $+3/-2.7$ LSBs on a 12 bit scale. The INL is much larger than expected, and is believed to be due to current source transistors entering the triode region due to larger BDC offsets than the design accommodated. Furthermore, as shown in the frequency response plots of Fig. 28, the dynamic range, SFDR, and SNDR were measured to be 72 dB (11.7 bits), 68 dB (11 bits), and 62 dB (10 bits) respectively. These parameters are also plotted versus the sampling frequency in Fig. 29. Fig. 30 plots the measured SNDR as a function of the input signal amplitude showing that the circuit noise limit is effectively 11.7 bit
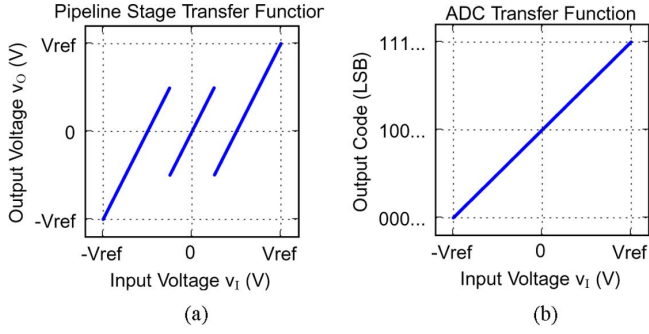
Fig. 31. Ideal stage voltage transfer function (a) and ADC transfer function (b) for a 1.5 bit/stage ADC.

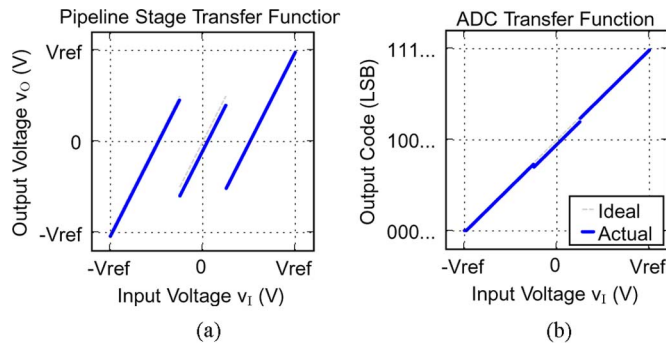Fig. 33. Differential ZCBC showing series ON-resistance of reference switches.

Fig. 32. Voltage transfer function (a) and ADC transfer function (b) for a 1.5 bit/stage ADC including series resistance mismatch for the voltage reference switches.

and that distortion of a full scale input signal limits the resolution to 10 bits. The figure of merit is 88 fJ/step. The results are summarized for two sampling rates in Table I.

IX. CONCLUSION

Since the dynamic range of this design is approximately 12 bit accurate and the SNDR is 10 bit accurate, this design is clearly limited by INL-induced distortion, and the dominant source of INL is from the large offset in the bit decision comparators. While there are many ways to improve the offset of the bit decision comparators, this is an area requiring future research and improvement. Obvious methods to consider include increased sizing, offset compensation, and/or pre-amplification. Other ways are to consider alleviating the offset burden of the BDCs by adding more over-range protection or developing ramp linearization techniques that require less output range than a cascoded current source.

This zero-crossing based ADC features a fully differential signalling path that requires no CMFB, power-efficient offset compensation via chopper offset estimation, and output range enhancement via additional redundancy. It represents a significant step forward in the resolution, performance, and robustness of zero-crossing based circuits and reaches state-of-the performance in terms of power efficiency.
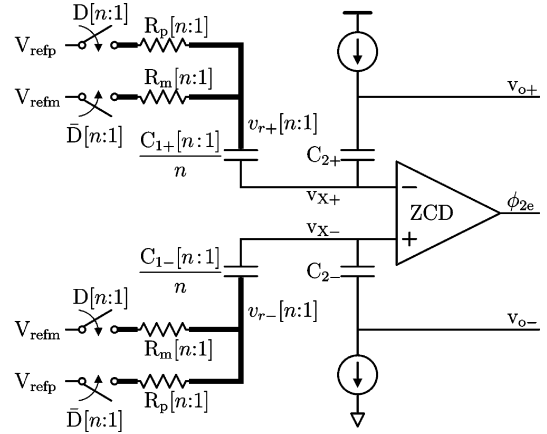
APPENDIX
REFERENCE SWITCH VOLTAGE DROPS

The schematic of Fig. 12 shows a traditional 1.5 bit/stage implementation in the transfer phase. The analog multiplexer selects between three voltage references. At the end of an ideal voltage transfer, the output voltage will have the form

$$v_o = 2v_i - v_r \tag{2}$$

where v_i is the voltage that was sampled on both capacitors during the sampling phase and v_r is the output of the reference voltage multiplexer. There are three different possible values for v_r that correspond to the three possible bit decision states, and each results in a corresponding different reference voltage selection. Suppose each switch to produces a voltage drop of Δ_p, Δ_c, and Δ_m corresponding to the switch associated with V_{refp}, V_{refcm}, and V_{refm} respectively. Solving for v_r under these three conditions yields

$$v_r = V_{\text{refp}} + \Delta_p \; \text{for} D[0] = 1 \& D[1] = 1$$
$$v_r = V_{\text{refcm}} + \Delta_c \; \text{for} D[0] = 1 \& D[1] = 0$$
$$v_r = V_{\text{refm}} + \Delta_m \; \text{for} D[0] = 0 \& D[1] = 0.$$

Substituting these into (2) gives the three possible output voltage states as

$$v_o = 2v_i - (V_{\text{refp}} + \Delta_p) \; \text{for} D[0] = 1 \& D[1] = 1$$
$$v_o = 2v_i - (V_{\text{refcm}} + \Delta_c) \; \text{for} D[0] = 1 \& D[1] = 0$$
$$v_o = 2v_i - (V_{\text{refm}} + \Delta_m) \; \text{for} D[0] = 0 \& D[1] = 0.$$

For these to produce a linear response, the center equation must subtract a quantity that is exactly the average of the outer two:

$$V_{\text{refcm}} + \Delta_c = \frac{1}{2}(V_{\text{refp}} + \Delta_p + V_{\text{refm}} + \Delta_m). \tag{3}$$

An ideal residue plot and complete ADC transfer function as shown in Fig. 31 is achieved when this constraint is satisfied. When this constraint is not satisfied, a response results like that of Fig. 32 where Δ_p, Δ_c, and Δ_m were given values of 2%, 10%, and 4% respectively. One can see in the complete ADC

transfer function that the center segment is misaligned due to the voltage drop mismatch.

When using capacitor splitting to eliminate the middle reference voltage as described in Section IV, the ideal voltage transfer takes the form

$$v_o = 2v_i - \frac{1}{2}(v_{r1} + v_{r2}) \qquad (4)$$

where v_{r1} and v_{r2} are the outputs of each multiplexer (see Fig. 13). Enumerating the possible values for v_{r1} and v_{r2} under the three different bit decision states gives

$$v_{r1} = V_{\text{refp}} + \Delta_p, v_{r2} = V_{\text{refp}} + \Delta_p,$$
$$\text{for } D[0] = 1, \quad D[1] = 1$$
$$v_{r1} = V_{\text{refm}} + \Delta_m, v_{r2} = V_{\text{refp}} + \Delta_p,$$
$$\text{for } D[0] = 1, \quad D[1] = 0$$
$$v_{r1} = V_{\text{refm}} + \Delta_m, v_{r2} = V_{\text{refm}} + \Delta_m,$$
$$\text{for } D[0] = 0, \quad D[1] = 0.$$

Substituting this result into (4) gives the output voltage under the three different states as

$$v_o = 2v_i - (V_{\text{refp}} + \Delta_p)$$
$$\text{for } D[0] = 1, \quad D[1] = 1$$
$$v_o = 2v_i - \frac{1}{2}(V_{\text{refp}} + \Delta_p + V_{\text{refm}} + \Delta_m)$$
$$\text{for } D[0] = 1, \quad D[1] = 0$$
$$v_o = 2v_i - (V_{\text{refm}} + \Delta_m)$$
$$\text{for } D[0] = 0, \quad D[1] = 0.$$

Now the voltage drop for the center equation is exactly the average of the other two, which means it satisfies the linearity constraint of (3) and produces an linear response.

Now consider the more general case of a fully differential implementation when n bit decision comparators are used in the implementation of a $\log_2(n+1)$ bit/stage ZCBC stage as shown in Fig. 33. Here the analog multiplexer has been implemented as the parallel combination of an ideal switch and a series resistor where R_p is the resistance of switches connecting to V_{refp} and R_m to V_{refm}. The iterative instance notation denotes parallel instantiations of multiple instances and wide wires denote buses of unique connections. As before, sampling capacitors $C_1\pm$ are split into n equal parts. The voltage on nodes $v_{r+}[i]$ to $v_{r-}[i]$ is the reference voltage that matters to the ZCBC. The output or residue voltage when an ideal transfer phase is realized can be calculated as

$$v_o = 2v_i - \frac{1}{n}\sum_{i=1}^{n} v_r[i] \qquad (5)$$

where the following differential voltage definitions have been used

$$v_o = v_{o+} - v_{o-}$$
$$v_i = v_{i+} - v_{i-}$$
$$v_r[i] = v_{r+}[i] - v_{r-}[i].$$

To analyze the effect of the series resistance, initially assume the current sources provide equal and opposite amounts of current so that the voltage drop across R_p and R_m can be expressed as Δ_p and Δ_m respectively. Furthermore, using the definitions

$$V_{\text{ref}} = V_{\text{refp}} - V_{\text{refm}}$$
$$\Delta = \Delta_p + \Delta_m,$$

the sum of each reference voltage $v_r[i]$ when k bits of bit decision vector $D[n:1]$ are high can be calculated as

$$\sum_{i=1}^{n} v_{ri} = (2k - n)V_{\text{ref}} + n\Delta. \qquad (6)$$

Substituting this result into (5) gives the residue voltage as

$$v_o = 2v_i - \left(\frac{2k}{n} - 1\right)V_{\text{ref}} - \Delta. \qquad (7)$$

Since k is the number of bit decisions comparators that switched high, the voltage drop is linearly interpolated for each sub-ADC decision level to produce a linear response with an offset of Δ.

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