A Fully-Differential Zero-Crossing-Based 1.2V 10b 26MS/s Pipelined ADC in 65nm CMOS

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Abstract

A fully-differential zero-crossing-based 10b 26MS/s pipelined ADC in a 65 nm CMOS process is presented. Switched-capacitor overshoot correction is compatible with the differential topology and allows faster operation. A CMFB is engaged in the coarse phase for constant common-mode. The 0.33mm^2 ADC achieves 54.3dB SNDR with a FOM of 161fJ/step.

ADC Implementation

Comparator-based switched-capacitor (CBSC) circuits were introduced as an alternative way to achieve low power and to overcome the design bottlenecks of op-amps [1]. Subsequently, a zero-crossing-based circuit (ZCBC) [2], in which comparators are replaced by dynamic zero-crossing detectors, achieved higher power efficiency and speed. These approaches, however, used single-ended architectures that were sensitive to supply and substrate noise. In this paper, a fully-differential zero-crossing based pipelined ADC is described. This differential architecture offers similar benefits to op-amp based differential ADCs.

The architecture of the proposed ADC based on fully-differential ZCBC is similar to the conventional ADC [3], consisting of Flash ADCs, MDACs, and digital correction logic (DCL). A load of replica MDAC is employed at the last stage to produce the same ramp rate as in other stages, because the ramp rate is a function of capacitive load. To avoid current consumption in the reference ladder in flash ADCs, a switched capacitor comparators [4] are used instead. The ADC is composed of 9 pipelined 1.5 bit stages. For simplicity of the design, Stages 2 through 9 are made identical. Stage 1 is made twice as large for lower noise. The schematics of the fully-differential ZCBC pipeline stages are shown in Fig. 1. It uses dual phase differential ramps for virtual ground detection by a zero-crossing detector (ZCD). Current sources I_1 and I_2 are for the coarse and the fine phases, respectively. Each current source is biased by a separate diode-connected current reference in order to maximize testability, at the cost of increased power consumption by a large factor.

The timing diagram is shown in Fig. 2. The input voltage is sampled on C_1, C_2, C_3, and C_4 prior to the beginning of charge-transfer phase (the rising edge of Q_1). A short preset signal P sets OUTT to GND and OUTC to VDD through SW_1 and SW_2. This ensures that the differential input to the ZCD is always negative at the start of the coarse phase. After the preset, the coarse charge-transfer phase E_1 begins. The coarse current I_1 charges OUTT and discharges OUTC at a fast rate until the inputs V_x and V_y cross each other. At this point, the

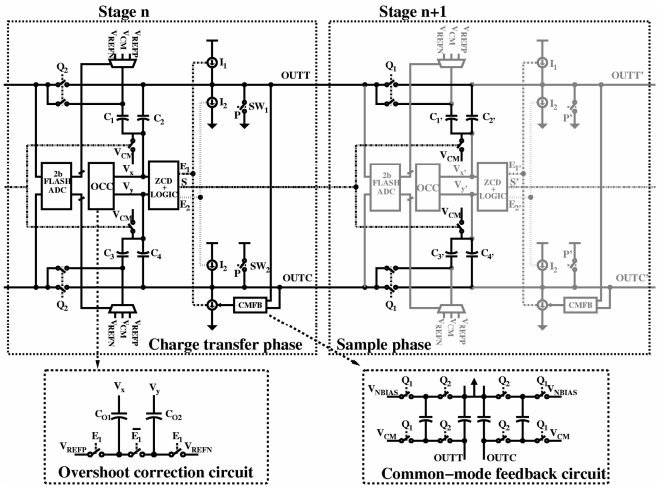

Fig. 1. Implementation of 2 stages of the fully differential ZCBC 1.5b/stage ADC.

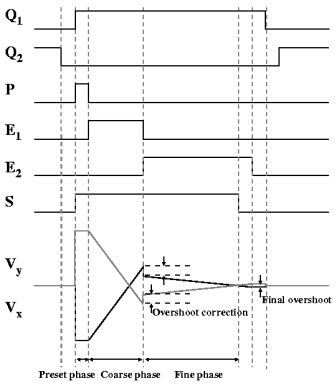

Fig. 2. Timing diagram.

ZCD makes its first decision. Because the ZCD has a finite delay, I_1 turns off shortly after V_x crosses V_y. The fast ramp rate and the finite delay in the ZCD causes overshoot during the coarse phase. In the previous work, an overshoot correction circuit with variable comparator threshold was used to reduce the overshoot voltage [1]. Since it is not straightforward to change the switching threshold of the fully-differential ZCD, a switched-capacitor overshoot correction circuit (OCC) has been implemented. C_{O1-2} are charged during the coarse phase, and the charge on C_{O1-2} is subtracted from C_1, C_2, C_3, and C_4 at the end of the coarse phase. This reduces the coarse phase overshoot, and maximizes the time for the fine phase for higher power efficiency without affecting the accuracy of the charge transfer at the end of the fine phase.

During the coarse phase, a switched-capacitor common-mode feedback (CMFB) shown in the inset of Fig. 1 is engaged to maintain a constant output common-mode. The CMFB is used only during the coarse phase because the output voltage changes are very small in the fine phase causing negligible common-mode variation. After I_1 turns off

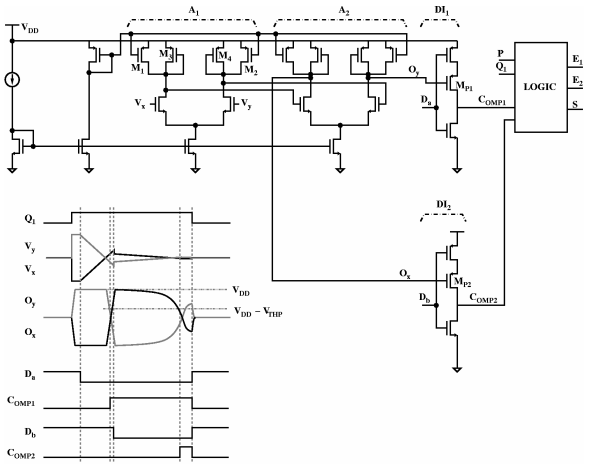

Fig. 3. Schematic of zero-crossing detector and timing diagram.

at the end of the coarse phase, current source I_2 turns on to begin the fine charge-transfer phase E_2. The current I_2 is much smaller than I_1 resulting in a slower ramp that generates much smaller overshoot [1]. When the inputs V_x and V_y cross again during the fine phase, the sampling signal S falls to open the sampling switches. The accurate output voltage is sampled on the next stage capacitors $C_{1'}$,$C_{2'}$,$C_{3'}$ and $C_{4'}$ at that instant. The final overshoot in the fine phase is constant and contributes a constant input referred offset in the ADC.

A single differential ZCD is used for both the fine phase and the coarse phase to reduce power consumption. The ZCD has two stages of differential amplifiers A_1 and A_2 followed by dynamic inverters DI_1 and DI_2 as shown in Fig. 3. The differential amplifier stages provide voltage gain and common-mode and power supply rejection. The first stage A_1 is a band-limited stage in order to control noise. The diode-connected loads $M_{3\text{-}4}$ are used to avoid explicit common-mode feedback. $M_{1\text{-}2}$ reduce the drain current of $M_{3\text{-}4}$ to increase gain. Since a dynamic inverter can detect only a negative-going change of the input signal, DI_1 and DI_2 are used during the coarse and fine phases, respectively. D_a and D_b are pre-charging signals for dynamic inverters DI_1 and DI_2. They make their decisions when their inputs O_y and O_x fall below their switching threshold. The switching threshold of DI_1 and DI_2 are maintained constant because their input waveforms O_y and O_x are invariant. The signals S, E_1, and E_2 are generated from the ZCDs' outputs $C_{OMP1\text{-}2}$ and signals P and Q_1 by combinational logic. When O_y falls below DI_1's threshold, the C_{OMP1} rises rapidly, finishing the coarse phase. At the start of the fine phase, D_b goes low and finishes precharging DI_2. M_{P2} waits until O_x falls below DI_2's threshold. After the output of DI_2 C_{OMP2} rises, the sampling signal S falls to take the sample of the output. E_2 turns off shortly after S goes down, turning off the fine phase current source. This ensures the linearity of the ramp until after the sample of the output is taken.

Experimental Results

A prototype fully-differential ZCBC pipeline ADC is fabricated in a 65nm 1.2V CMOS process. The active die area of the ADC excluding bias block and test circuits is 0.33mm^2 as shown in Fig. 4. The measured results of the ADC are shown in Fig. 5. The DNL and INL are +0.16/-0.22LSB and

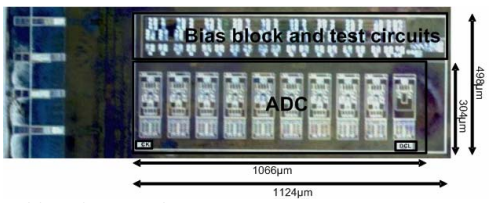

Fig. 4. Chip micrograph.

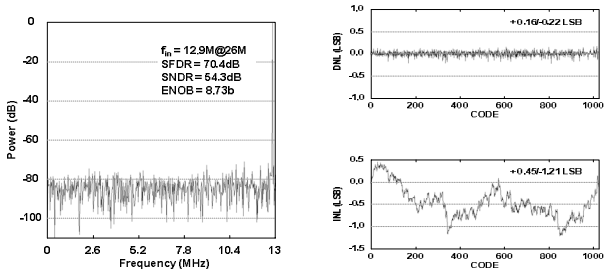

Fig. 5. Measured output spectrum, DNL, and INL.

+0.45/-1.21LSB, respectively. The SNDR with a 12.9MHz input tone, is 54.3dB (8.73 ENOB), and the SFDR is 70.4dB. Table I shows the performance summary. The core ADC power consumption excluding the bias block and test circuits is 1.78mW, resulting in a 161fJ/step FOM. As explained previously, the bias block is designed for maximum test flexibility at the cost of substantial increase in power consumption. The power consumption of the bias block is 3.73mW, which can be significantly reduced by not synthesizing the bias voltages individually for the various stages and by employing bypass capacitors at the bias nodes. Even when the excessively high power consumption of the bias block is included, the resulting FOM is 499fJ/step.

References

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TABLE I. Performance Summary

Technology	65nm CMOS 1-Poly 6-Metal
Supply voltage	1.2V
Resolution	10b
Sampling frequency	26MS/s
Full-scale analog	1.0Vpp
Die area	0.33[*1]mm^2 / 0.56[*2]mm^2
Power consumption	1.78[*1]mW / 5.51[*2]mW
DNL	+0.16 / -0.22LSB
INL	+0.45 / -1.21LSB
ENOB	8.73b
FOM	0.161[*1]pJ/step / 0.499[*2]pJ/step

[*1] : ADC Core only
[*2] : Including bias and test blocks